HIGH SPEED DATA PROCESSING INTEGRATED CIRCUIT HANDBOOK

PLESSEY
Semiconductors

Designed and produced by Peter Wigens Consultants

February 1983
Publication No. P.S. 1989

Contents

Product Index

* The SP16F60, SP16F70, SP9131, SP9685 and SP9687 are pin-compatible higher performance versions of the equivalents shown.

Quality data

Plessey Semiconductors has Factory Approval to:-

BS9300 for semiconductor devices of Assessed Quality (BSI Certificate 1053/M)

BS9400 for integrated circuits of Assessed Quality (BSI Certificate 1053/M)

CECC 50000 Inspection Organisation to document level 1 (BS9300) M0020/CECC refers

DEF STAN 05 — 21 QC System requirements for Industry (Equivalent to AQAP — 1) Certificate 65752/1/01 refers

Devices are also manufactured and tested in accordance with the methods of **MIL-STD-833**, the US Military Standard; Test Methods and Procedures for Microcircuits, and **MIL-M-38510**, US Military Specification, Micro-electronics; General Specifications for.

Ordering information

All Plessey Semiconductors integrated circuits are allocated type numbers which must be quoted when ordering. This number may or may not have a suffix (A, B, C, etc.) which denotes the precise electrical specification or temperature grade. When there is a choice of packages the two-digit Pro-Electron code is used to identify the style required, according to the following table:

CM - Multilead TO-5
DC - Ceramic Dual-in-Line (metal lid)
DG - Ceramic Dual-in-Line

Within the UK, orders for quantities up to 99 will be referred to your local Distributor. Quantities of 1000 and over must be ordered from:

Plessey Semiconductors Limited
Cheney Manor
Swindon, Wiltshire SN2 2QW
United Kingdom
Telephone: Swindon (0793) 36251
Telex: 449637

A reciprocal arrangement exists with all Distributors, but it will expedite delivery of order if buyers can direct orders as indicated above. Outside the UK, irrespective of quantity, you are invited to contact your nearest Plessey Semiconductors Sales Outlet (see pp. 109-111).

DELIVERED PRODUCT QUALITY

It is our policy to deliver a reliable quality product and to achieve this end all devices undergo 100% electrical testing of every relevant AC and DC parameter prior to shipment. The devices are tested under conditions of level and frequency closely simulating those of the typical application. Fully automatic Teradyne integrated circuit test machines, acknowledged to be among the best computer controlled test machines available, are employed.

Each and every stage of processing, assembly and testing is carefully audited by Plessey Semiconductors' independent Quality Assurance department.

Therefore we are able to guarantee the following Acceptable Quality Level (A.Q.L.) on all deliveries.

MECHANICAL

Defects of a mechanical nature including coding not being legible, deformed leads, dimensional tolerances being exceeded, wrong identification of pin 1 and pins not being solderable.

0.65 %AQL, I.L. II

ELECTRICAL

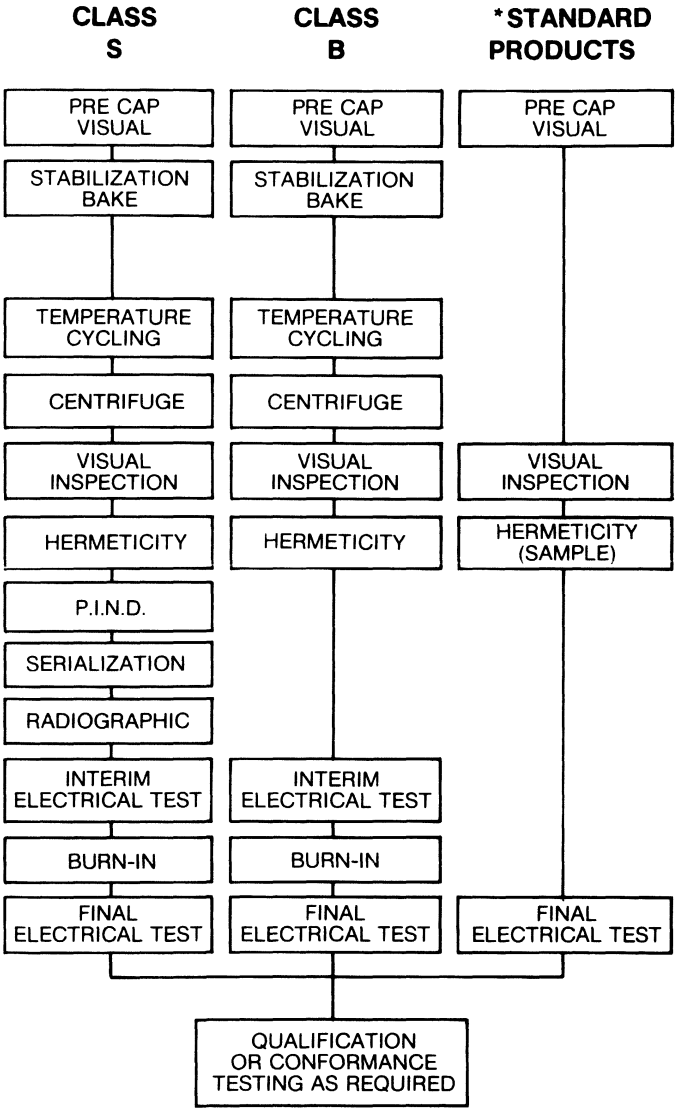
Defects of an electrical nature including device parameters being outside the acceptance specification limits,or those only stated as typical being grossly in error.

0.4 %AQL, I.L. II

The average delivered product quality is considerably better than this, the population of imperfect devices being much smaller than that indicated by the AQL values.

Screening to MIL-STD-883

The following Screening Procedures are available from Plessey Semiconductors



*Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

Semi-custom design

The table outlines the essential parameters of our Semi-custom design techniques, including typical timescales for the design and production of a Semi-custom IC.

NAME	PART NUMBER	TECHNOLOGY	LOGIC ELEMENTS	TYP.GATE DELAY/POWER	SYSTEM CLOCK SPEED
Microcell	MJ 1XXX	NMOS (Std)	Up to 3000 equiv.gates	50ns at 250μW	2MHz
	MJ 1XXX	NMOS (low power)	Up to 3000 equiv.gates	200ns at 40μW	2MHz
	MV 1XXX	CMOS	Up to 2000 equiv.gates	20ns at 12μW/MHz	8MHz
Microgate-C 1000 Series (CMOS Gate Array)	CLA 10XX	CMOS	560	6ns at 6μW/MHz	8MHz
	CLA 12XX	CMOS	960	6ns at 6μW/MHz	8MHz
	CLA 15XX	CMOS	1440	6ns at 6μW/MHz	8MHz
Microgate-C 2000 Series (CMOS Gate Array)	CLA 21XX	CMOS	840	4ns at 3μW/MHz	14MHz
	CLA 23XX	CMOS	1440	4ns at 3μW/MHz	14MHz
	CLA 25XX	CMOS	2400	4ns at 3μW/MHz	14MHz
Microgate-E (ECL Gate Array)	SCD 1XXX	ECL	75	550ps/900mW	300MHz
	SCD 2XXXH	ECL	300	550ps/3.5W	300MHz
	SCD 2XXXM	ECL	300	1.5ns/1W	250MHz
	SCD 2XXXL	ECL	300	2ns/750mW	100MHz

NAME	PART NUMBER	TECHNOLOGY	COMPONENT COUNT		
			RESISTANCE	TRANSISTORS	
				NPN	PNP
Microlin (Analogue Array)	BAA 1XXX	Bipolar	1219kΩ	81	28
	BAA 2XXX	Bipolar	2757kΩ	163	58

*Design and test times given are typical. Actual times will depend on the complexity of the particular circuit.

INPUT/ OUTPUT ELEMENTS	COMPATI-BILITY	MAX. PIN COUNT	No. OF CUSTOM MASKS	TYPICAL TIME FOR 1st SAMPLES
As required	TTL/CMOS	64	6	19 weeks *
As required	TTL/CMOS	64	6	
As required	TTL/CMOS	64	9	
38 I or O	TTL/CMOS	40	1	16 weeks *
50 I or O	TTL/CMOS	64	1	
60 I or O	TTL/CMOS	64	1	
40 I or O	TTL/CMOS	44	3	13 weeks *
52 I or O	TTL/CMOS	56	3	
60 I or O	TTL/CMOS	64	3	
25 I or O	ECL 10K	28	3	16 weeks *
36 I 20 I or O	ECL 10K	64	3	
36 I 20 I or O	ECL 10K	64	3	
36 I 20 I or O	ECL 10K	64	3	

f_T (1mA 5V Vcc) STANDARD NPN	LV_{CEO}/ BV_{CEO}	MAX. PIN COUNT	No. OF CUSTOM MASKS	TYPICAL TIME FOR 1st SAMPLES
470MHz	20V/30V	24	1	15 weeks *
470MHz	20V/30V	24	1	

Technical Data

NOTE

ECL power supplies are nominally +5V, -5.2V unless stated otherwise. Supply tolerance of ±0.25V will give correct functional operation. Electrical characteristics are measured at nominal supplies.

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SP705B

CRYSTAL CONTROLLED INTEGRATED CIRCUIT OSCILLATOR

The SP705B is a square wave oscillator circuit designed to operate in conjunction with an AT cut quartz crystal of effective series resistance less than 300 ohms. Four TTL outputs are provided, related in frequency to the crystal frequency f as follows: $f/2$, $f/4$, $\overline{f/2}$ and $\overline{f/4}$. The SP705B is therefore ideally suited to either single or multi-phase TTL clock applications.

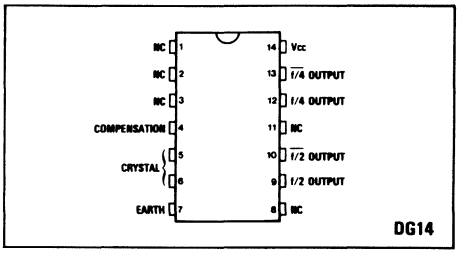

Fig.1 Pin connections

FEATURES

- Operating Frequency up to 10MHz
- f/2 and f/4 Outputs
- 4 TTL Level Outputs
- Operates from +5V TTL Supply

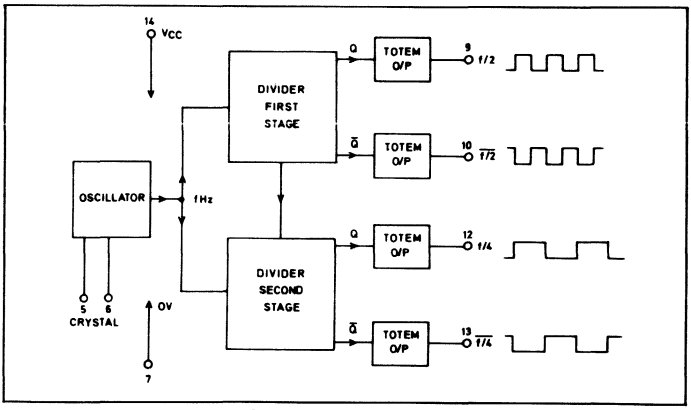

Fig.2 SP705B block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = +5V

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
High state output voltage	V_{OH}	2.6		V	V_{CC} = 4.75V I_{OH} = 0.2mA
Low state output voltage	V_{OL}		0.4	V	V_{CC} = 5.25V I_{OL} = 8mA
Supply current	I_{CC}		35	mA	V_{CC} = 5V
Output rise time (10 % to 90 %)	t_R		20	ns	V_{CC} = 5V
Output fall time (90 % to 10 %)	t_F		20	ns	V_{CC} = 5V
Operating frequency (f)			10	MHz	
Operating temperature range		0	70	°C	

CIRCUIT DESCRIPTION

The crystal maintaining circuit consists of an emitter-coupled oscillator, with the emitter resistors replaced by constant-current generators. The crystal is connected, usually in series with a 20pF capacitor, between pins 5 and 6. The 20pF capacitor can be replaced with a mechanical trimmer to allow small changes in frequency to be made, as shown in Fig.3.

The circuit is designed to provide low crystal drive levels - typically, less than 0.15mW at 5MHz. This is well within crystal manufacturers' limit of 0.5mW.

The compensation point, pin 4 is made available so that the compensation capacitance can be increased if necessary. However the 14pF capacitor included on the chip is usually sufficient to prevent spurious oscillation at high frequencies.

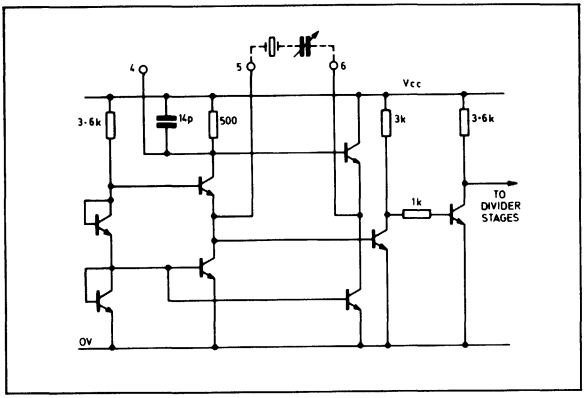

Fig.3 Circuit diagram of SP705B oscillator

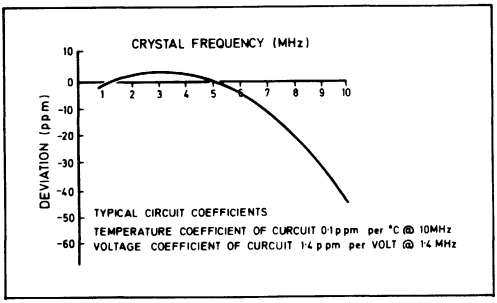

Fig.4 Deviation from nominal crystal frequency

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SP1648

VOLTAGE-CONTROLLED OSCILLATOR

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with ECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The device may also be used in phase locked loops and many other applications requiring a fixed or variable frequency clock source of high spectral purity.

The SP1648 may be operated from a +5.0 Vdc supply or a −5.2 Vdc supply, depending upon system requirements.

SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
−5.2 Vdc	1, 14	7, 8

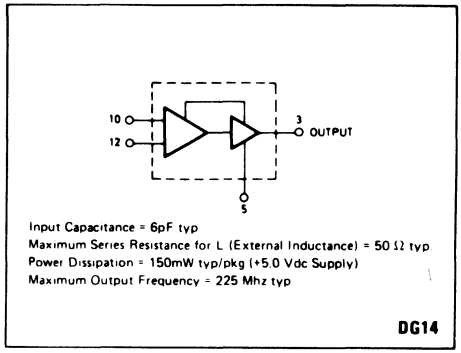


Fig. 1 Block diagram of SP1648

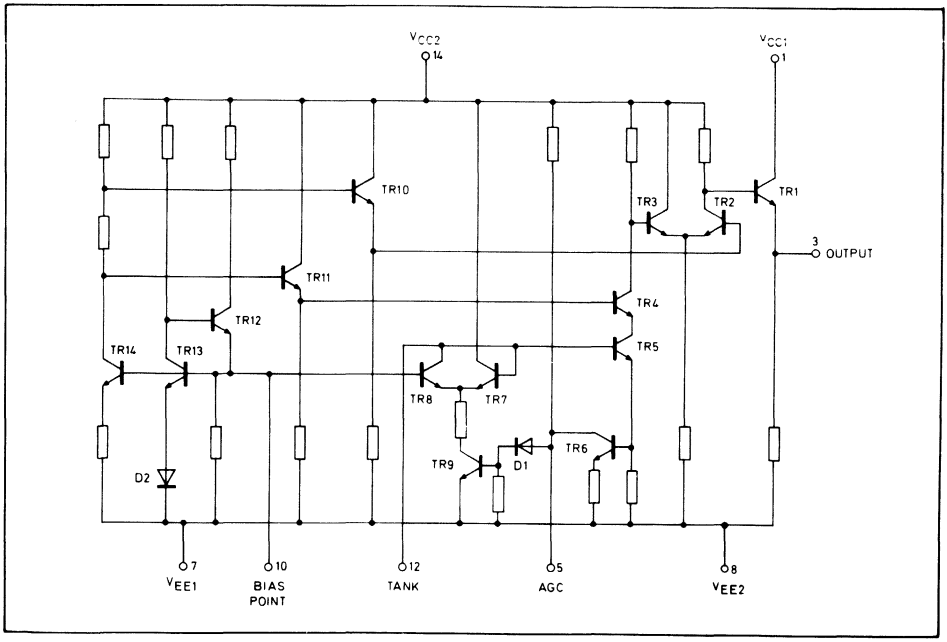


Fig. 2 Circuit diagram of SP1648

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply Voltage = +5.0 volts

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	mAdc I_L
-30°C	+1.960	+1.410	5.0	5.0
+25°C	+1.800	+1.300	5.0	5.0
+85°C	+1.680	+1.180	5.0	5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	I_L	V_{EE} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	40	—	—	mAdc	—	—	1, 14	—	7, 8
Logic "1" Output Voltage	V_{OH}	3	3.94	4.18	4.04	4.25	4.11	4.36	Vdc	—	12	1, 14	3	7, 8
Logic "0" Output Voltage	V_{OL}	3	3.16	3.40	3.20	3.43	3.23	3.46	Vdc	12	—	1, 14	3	7, 8
Bias Voltage	V_{Bias}*	10	1.51	1.86	1.40	1.70	1.28	1.58	Vdc	—	—	1, 14	—	7, 8
			Min	Typ Max	Min	Typ Max	Min	Typ Max						
Peak-to-Peak Tank Voltage	V_{p-p}	12	—	— —	—	500 —	—	— —	mV	See Figure 4	—	1, 14	3	7, 8
Output Duty Cycle	V_{DC}	3	—	— —	—	50 —	—	— —	%	See Figure 4	—	1, 14	3	7, 8
Oscillation Frequency	f_{max}	—	—	— —	200	225 —	—	— —	MHz	See Figure 4	—	1, 14	3	7, 8

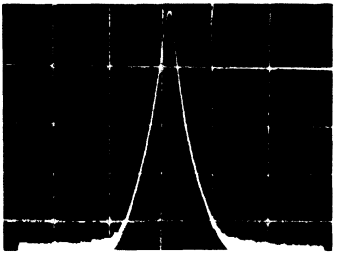
*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point

Supply Voltage = –5.2 volts

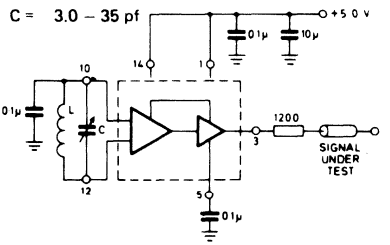
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	mAdc I_L
-30°C	-3.240	-3.790	-5.2	-5.0
+25°C	-3.400	-3.900	-5.2	-5.0
+85°C	-3.520	-4.020	-5.2	-5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	61	—	—	mAdc	—	—	7, 8	—	1, 14
Logic "1" Output Voltage	V_{OH}	3	-1.045	-0.815	-0.960	-0.750	-0.890	-0.650	Vdc	—	12	7, 8	3	1, 14
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	12	—	7, 8	3	1, 14
Bias Voltage	V_{Bias}*	10	-3.690	-3.340	-3.800	-3.500	-3.920	-3.620	Vdc	—	—	7, 8	—	1, 14
			Min	Typ Max	Min	Typ Max	Min	Typ Max						
Peak-to-Peak Tank Voltage	V_{p-p}	12	—	— —	—	500 —	—	— —	mV	See Figure 4	—	7, 8	3	1, 14
Output Duty Cycle	V_{DC}	3	—	— —	—	50 —	—	— —	%	See Figure 4	—	7, 8	3	1, 14
Oscillation Frequency	f_{max}	—	—	— —	200	225 —	—	— —	MHz	See Figure 4	—	7, 8	3	1, 14

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point

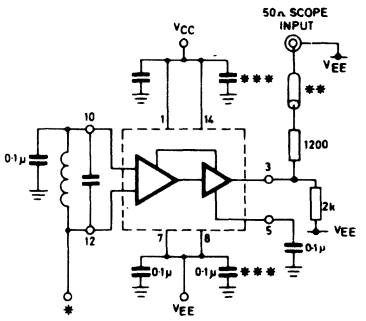


B.W. = 10kHz
Center Frequency = 100MHz
Scan Width = 50kHz/div
Vertical Scale = 10db/div



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe.

Fig. 3 Spectral purity of signal at output



* Use high impedance probe (>1.0 Megohm must be used).

** The 1200 -ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe.

*** Bypass only that supply opposite ground.

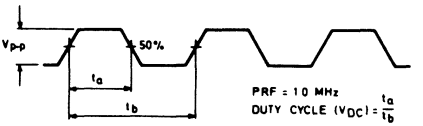


Fig. 4 Test circuit and waveforms

OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor TR7 to the collector of TR8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (TR7 and TR8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (TR4) is used to translate from the emitter follower (TR5) to the output differential pair TR2 and TR3. TR2 and TR3, in conjunction with output transistor TR1, provide a highly buffered output which produces a square wave. Transistors TR10 thru TR14 provide this bias drive for the oscillator and output buffer. Figure 3 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 5), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} ($\approx$ 1.4 V for positive supply operation).

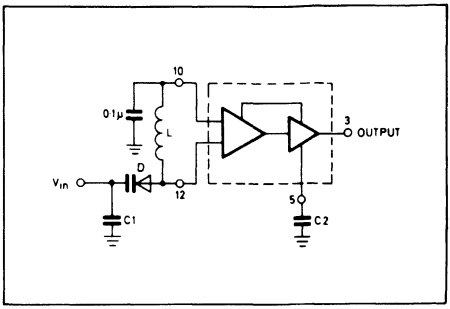
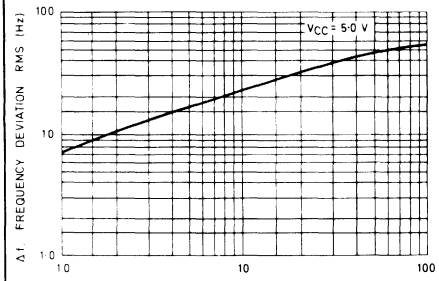


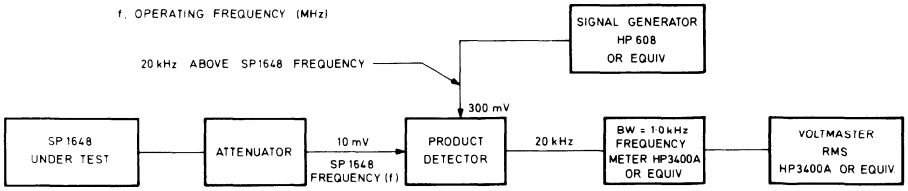
Fig. 5 The SP1648 operating in the voltage-controlled mode

When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 6.



OSCILLATOR TANK COMPONENTS
(CIRCUIT OF FIGURE 5)

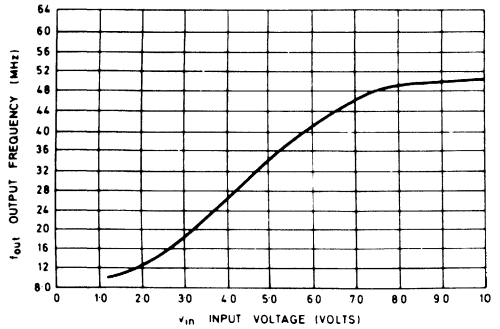
f MHz	D	L µH
1·0 - 10	MV 2115	100
10 - 60	MV 2115	2·3
60 - 100	MV 2106	0·15

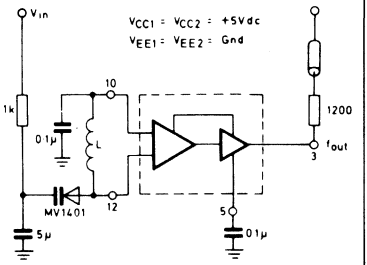


$$\text{FREQUENCY DEVIATION} = \frac{\text{(HP5210A OUTPUT VOLTAGE) (FULL SCALE FREQUENCY)}}{\text{1·0 VOLT}}$$

Note: Any frequency deviation caused by the signal generator and SP1648 power supply should be determined and minimised prior to testing.

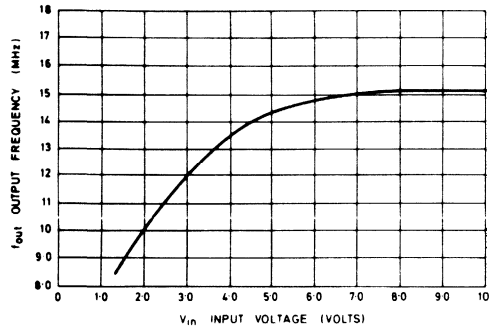
Fig. 6 Frequency deviation test circuit

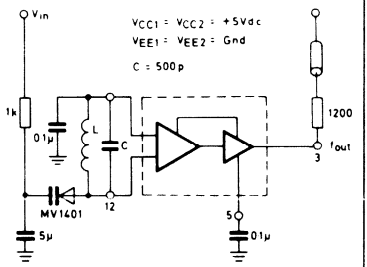




* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe.

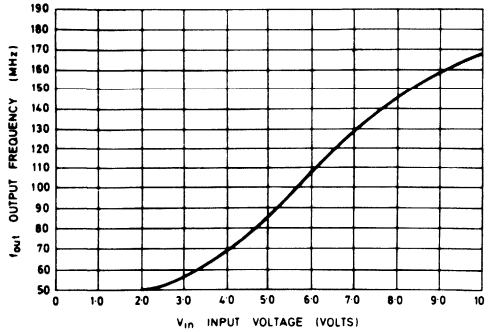
Fig. 7

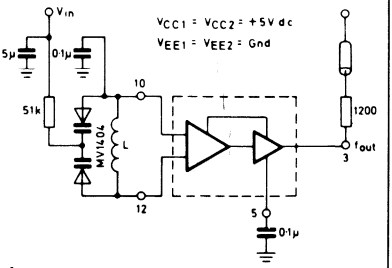




* The 1200 ohm resistor and the scope termination impedance consitute a 25:1 attenuator probe.

Fig. 8





* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe.

Fig. 9

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 7, 8, and 9. Figures 7 and 9 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of of the oscillator, 6pF typical). Figure 8 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 7 and 8 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 9 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D(max) + C_S}}{\sqrt{C_D(min) + C_S}}$$

where $f_{min} = \dfrac{1}{2\pi\sqrt{L\,(C_D(max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency by-passing is necessary on the power supply pins (see Figure 3).

Capacitors (C1 and C2 of Figure 5) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, −5.2 volts if a negative supply is used).

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a −5.2 volt supply is used).

PLESSEY
Semiconductors

SP1650

DUAL A/D COMPARATOR

The SP1650 is a very high speed comparator utilising differential amplifier inputs to sense analogue signals above or below a reference level. An output latch provides a unique sample-hold feature.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock iinputs ($\overline{C_a}$ and $\overline{C_b}$) operate from ECL III or ECL 10,000 digital levels. When $\overline{C_a}$ is at a logic high level, Q_a will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q_a}$ is the logic complement of Q_a. When the clock in to a low logic level, the outputs are latched in their present state.

FEATURES

- P_D = 330mW typ/pkg (No Load)
- t_{pd} = 3.5ns typ.
- Input Slew Rate = 350V/us
- Differential Input Voltage: -5.0V to +5.0V (-30°C to +85°C)
- common Mode Range: -3.0V to +2.5V (-30°C to +85°C)
- Resolution: ≤ 20mV (-30°C to +85°C)
- Drives 50Ω lines

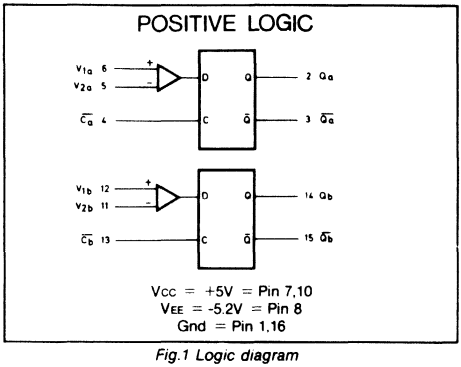


Fig.1 Logic diagram

TRUTH TABLE

C	V_1 V_2	Qn + 1	$\overline{Qn}$ + 1
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	Qn	$\overline{Qn}$

ϕ = Don't Care

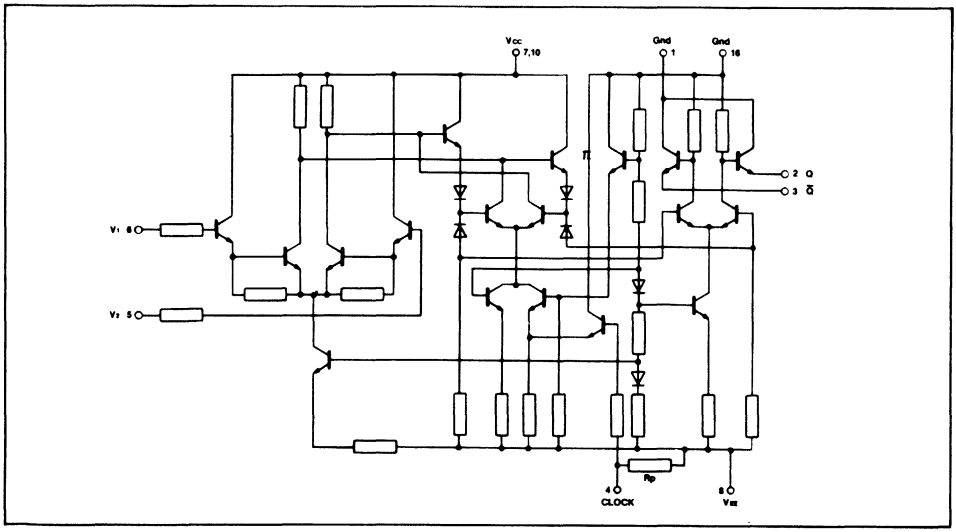


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to —2.0 Vdc.

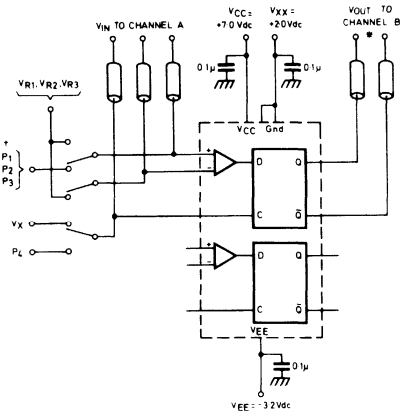
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020	See Note ④				+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

Characteristic	Symbol	Pin Under Test	SP1650 Test Limits (1) -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③	Gnd
Power Supply Drain Current																						
Positive	I_{CC}	7,10				25*			mAdc		4,13			6,12						7,10	8	1,5,11,16
Negative	I_E	8				55*			mAdc	4,13				6,12						7,10	8	1,5,11,16
Input Current	I_{in}	6				10			μAdc	4	13			12		6				7,10	8	1,5,11,16
Input Leakage Current	I_R	6				7			μAdc	4	13			12				6		7,10	8	1,5,11,16
Input Clock Current	I_{inH}	4				350			μAdc	4	13			6,12						7,10	8	1,5,11,16
	I_{inL}	4			0.5				μAdc		13			6,12						7,10	4.8	1,5,11,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4,13				6,12						7,10	8	1,5,11,16
		2													5,11							1,6,12,16
		2														6,12	5,11					1,16
		2																5,11	6,12			1,16
		3													6,12							1,5,11,16
		3												5,11								1,6,12,16
		3														5,11	6,12					1,16
		3																6,12	5,11			1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4,13					6,12					7,10	8	1,5,11,16
		2												5,11								1,6,12,16
		2														5,11	6,12					1,16
		2																6,12	5,11			1,16
		3												6,12								1,5,11,16
		3													5,11							1,6,12,16
		3														6,12	5,11					1,16
		3																5,11	6,12			1,16
Logic "1" Threshold Voltage ②	V_{OHA}	1																				
		2	-1.065		-0.980		-0.910		Vdc		13	4		6						7,10	8	1,5,16
		3											4		6							
		4										4			6							
		3											4	6								
Logic "0" Threshold Voltage ②	V_{OLA}	1																				
		2																				
		3		-1.630		-1.600		-1.555	Vdc		13	4		6						7,10	8	1,5,16
		2											4		6							
		4										4										
		2											4	6								

NOTES
1. All data is for ½ SP1650 except data marked (*) which refers to the entire package.
2. These tests done in order indicated. See Figure 6.
3. Maximum Power Supply Voltages (beyond which device life may be impaired): $|V_{EE}| + |V_{CC}| < 12V$ dc.
4. At all temperatures, $V_{A3} = +3.000V$, $V_{A4} = +2.980V$, $V_{A5} = -2.500V$ and $V_{A6} = -2.480V$.

Characteristic	Symbol	Pin Under Test	SP1650 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①	See Figure 4 P1	P2	P3	P4
										-30°C	+2.000	See Note ④		+1.040	+2.00	+7.00	-3.20				
										+25°C	+2.000			+1.110	+2.00	+7.00	-3.20				
										+85°C	+2.000			+1.190	+2.00	+7.00	-3.20				
											TEST VOLTAGE APPLIED TO PINS LISTED BELOW										
Switching Times																					
Propagation Delay	t_{6+2+}	2	2.0	5.0	2.0	5.0	2.0	5.7	ns		5	–	–	4	1,11,16	7,10	8	6	–	–	–
(50% to 50%)	t_{6+2+}	2									–	5	–					–	6	–	–
V-Input to Output	t_{6+2+}	2									–	–	5					–	–	6	–
	t_{6+3-}	3									5	–	–					6	–	–	–
	t_{6+3-}	3									–	5	–					–	6	–	–
	t_{6+3-}	3									–	–	5					–	–	6	–
	t_{6-2-}	2									5	–	–					6	–	–	–
	t_{6-2-}	2									–	5	–					–	6	–	–
	t_{6-2-}	2									–	–	5					–	–	6	–
	t_{6-3+}	3									5	–	–					6	–	–	–
	t_{6-3+}	3									–	5	–					–	6	–	–
	t_{6-3+}	3									–	–	5					–	–	6	–
Clock to Output ②	t_{4+2+}	2	2.0	4.7	2.0	4.7	2.0	5.2	ns		5	–	–	–	1,11,16	7,10	8	6	–	–	4
	t_{4+2-}	2									6	–	–	–				5	–	–	
	t_{4+3+}	3									6	–	–	–				5	–	–	
	t_{4+3-}	3									5	–	–	–				6	–	–	
Clock Enable Time ③	t_{setup}	6	–	–	2.5	–	–	–	ns		5	–	–	–	1,11,16	7,10	8	6	–	–	4
Clock Aperture Time ③	t_{ap}	6	–	–	1.5	–	–	–	ns		5	–	–	–	1,11,16	7,10	8	6	–	–	4
Rise Time	t_{2+}	2	1.0	3.5	1.0	3.5	1.0	3.8	ns		5	–	–	4	1,11,16	7,10	8	6	–	–	–
(10% to 90%)	t_{3+}	3	1.0	3.5	1.0	3.5	1.0	3.8	ns		5	–	–	4	1,11,16	7,10	8	6	–	–	–
Fall Time	t_{2-}	2	1.0	3.0	1.0	3.0	1.0	3.3	ns		5	–	–	4	1,11,16	7,10	8	6	–	–	–
(10% to 90%)	t_{3-}	3	1.0	3.0	1.0	3.0	1.0	3.3	ns		5	–	–	4	1,11,16	7,10	8	6	–	–	–

NOTES
1. Maximum Power Supply Voltages (beyond which device life may be impaired):
   $|V_{CC}| + |V_{EE}| = 12V$ dc.
2. Unused clock inputs may be tied to ground.
3. See Figure 10.
4. At all temperatures, $V_{R2} = +4.900V$ and $V_{R3} = -0.400V$.



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

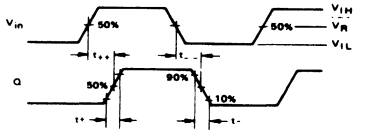
†Refer to Fig. 4 for input pulse definitions.

* Complement of output under test should always be loaded with 50ohms to ground

Fig. 3 Switching time test circuit at +25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V – Input to Output

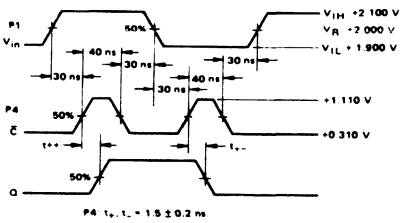


Test pulses: $t_+, t_- = 1.5 \pm 0.2$ ns (10% to 90%)
f = 5.0 MHz
50% Duty Cycle
V_{IH} is applied to $\bar{C}$ during tests

TEST PULSE LEVELS

	Pulse 1	Pulse 2	Pulse 3
V_{IH}	+2.100V	+5.000V	-0.300V
V_R	+2.000V	+4.900V	-0.400V
V_{IL}	+1.900V	+4.800V	-0.500V

Clock to Output



P4: $t_+, t_- = 1.5 \pm 0.2$ ns

Fig. 4 Switching and propagation waveforms @ 25°C

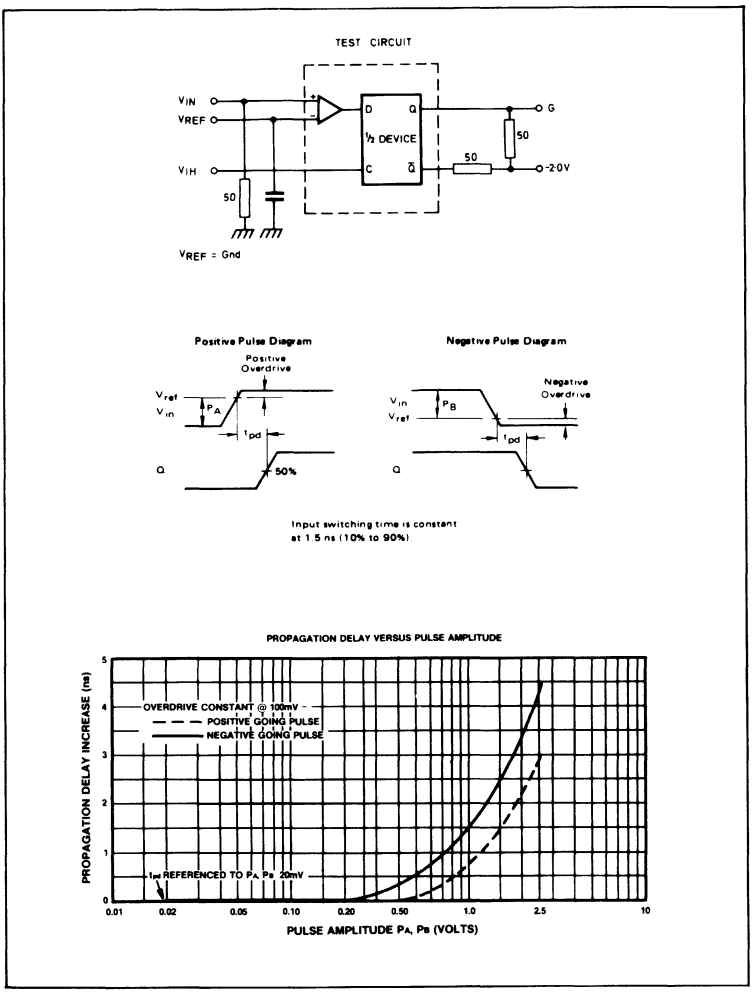


Fig. 5 Propagation delay (t_{pd}) v. input pulse amplitude and constant overdrive

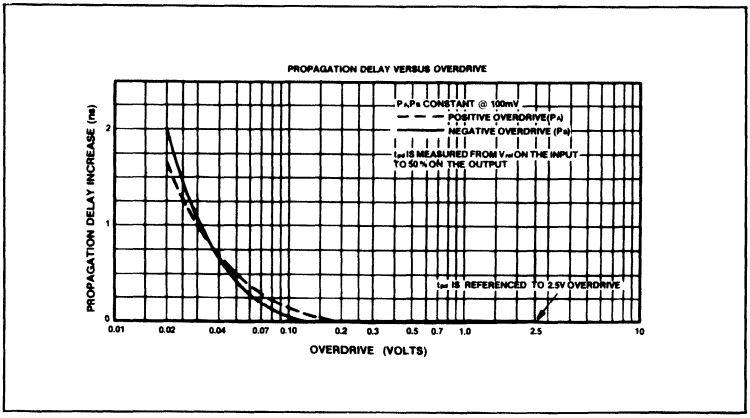


Fig. 5 (continued)

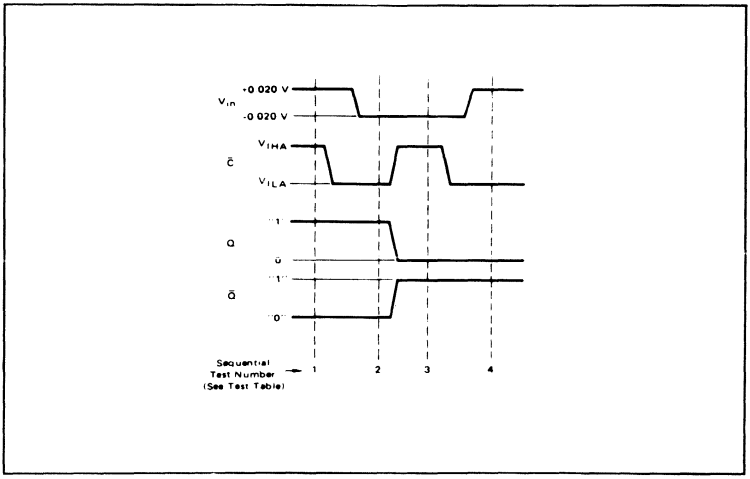


Fig. 6 Logic threshold tests (waveform sequence diagram)

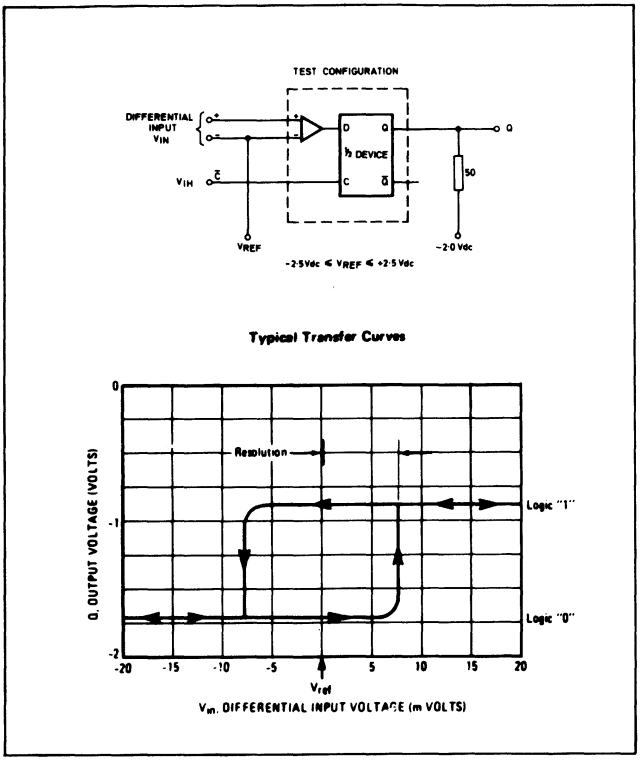


Fig. 7 Transfer characteristics (Q v. V_{in})

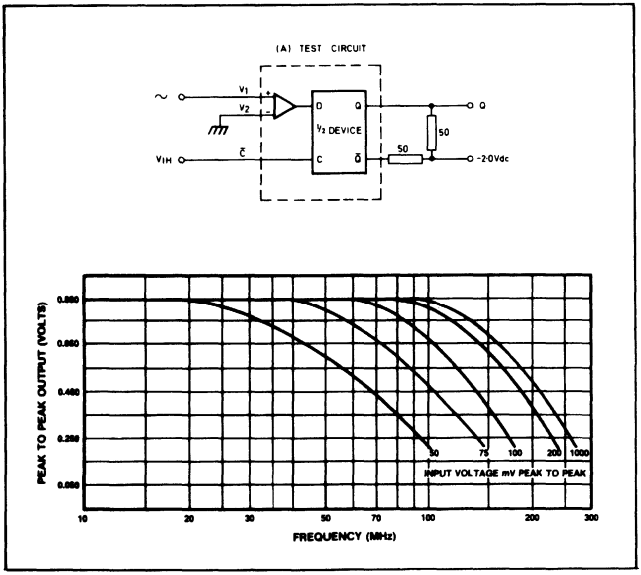


Fig. 8 Output voltage swing v. frequency

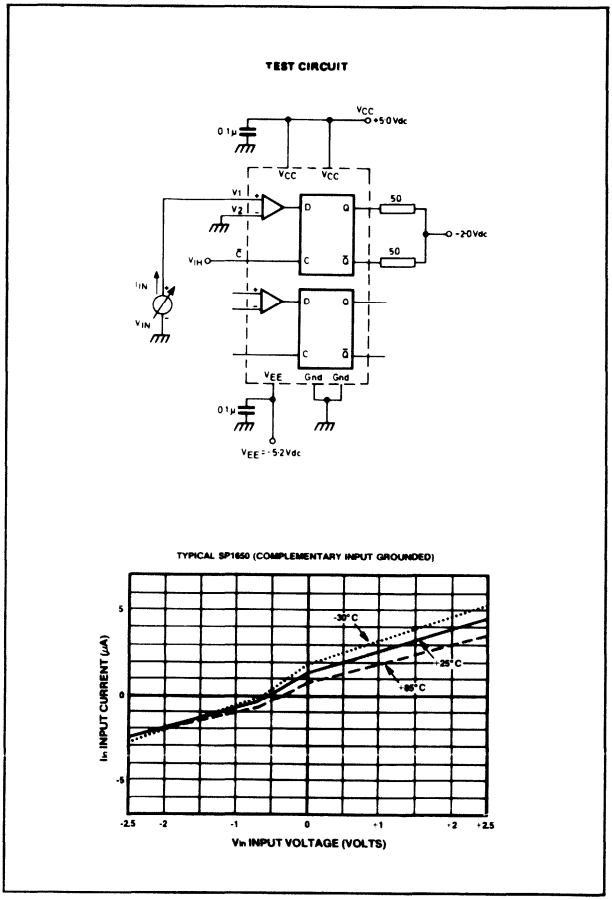
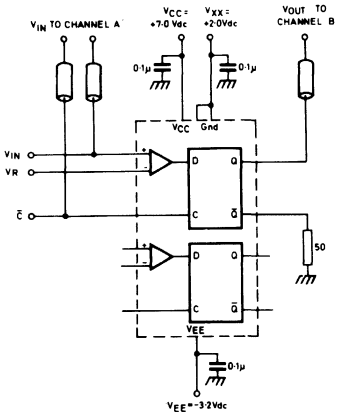


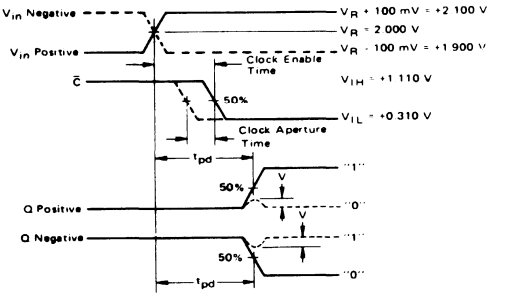
Fig. 9 Input current v. input voltage



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Analog Signal Positive and Negative Slew Case



——— Clock enable time=minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200ps.

- - - - - Clock aperture time=time difference between clock enable time and time that output does not switch and V is less than 150 mV.

Fig. 10 Clock enable and aperture time test circuit and waveforms @ 25°C

PLESSEY
Semiconductors

SP1658

VOLTAGE-CONTROLLED MULTIVIBRATOR

The SP1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with ECL III and ECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

The SP1658 is useful in phase-locked loops, frequency synthesizer and clock signal generation applications for instrumentation, communication, and computer systems.

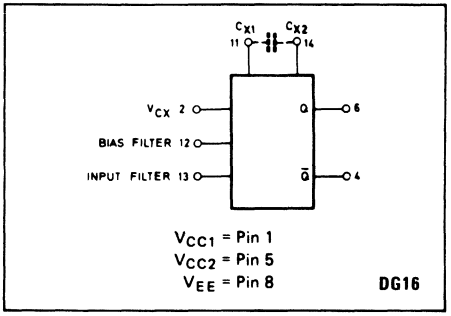


Fig. 1 Block diagram of SP1658

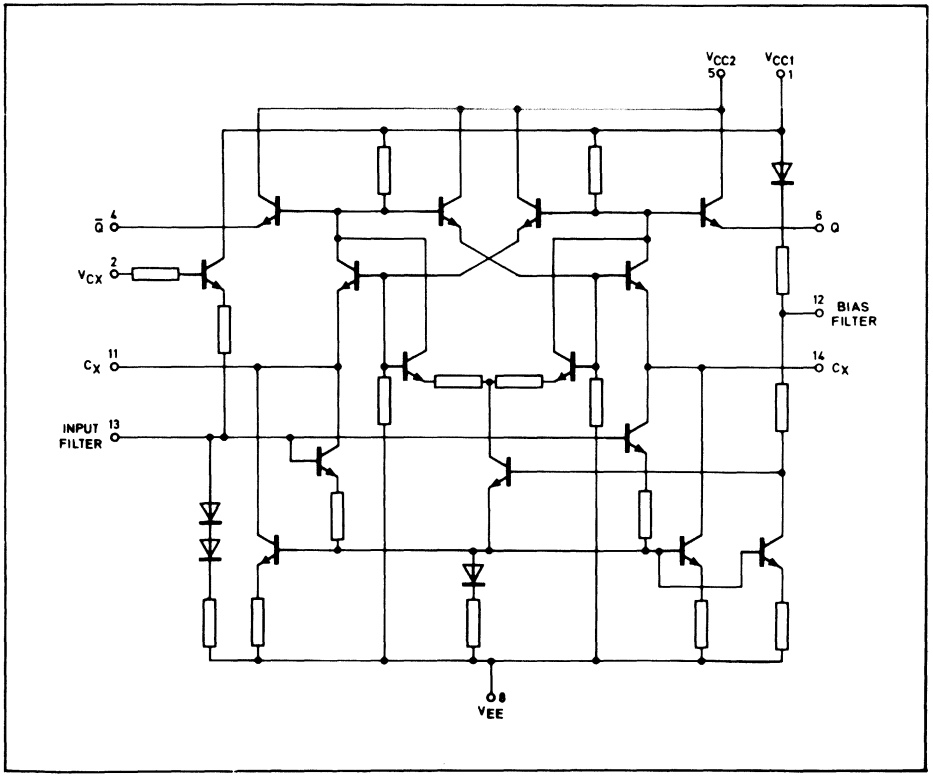


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES Vdc ±1% V_{IH}	V_{IL}	V_3	V_{EE}
-30°C	0.0	-2.0	-1.0	-5.2
+25°C	0.0	-2.0	-1.0	-5.2
+85°C	0.0	-2.0	-1.0	-5.2

Characteristic	Symbol	Pin Under Test	SP1658 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH}	V_{IL}	V_3	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8*	–	–	–	–	32	–	–	mAdc	2	–	–	8	1,5
		8**	–	–	–	–	32	–	–	mAdc	2	–	–	8	1,5
Input Current	I_{inH}	2*	–	–	–	–	350	–	–	µAdc	2	–	–	8	1,5
Input Leakage Current	I_{inL}	2*	–	–	-0.5	–	–	–	–	µAdc	–	2	–	8	1,5
High Output Voltage (OR)	V_{OH}	4**	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	2	8	1,5
		6*	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	2	8	1,5
Low Output Voltage (OR)	V_{OL}	4*	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	–	–	2	8	1,5
		6**	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	–	–	2	8	1,5
AC Characteristics (Figure 2) (Tests shown for one output, but checked on both)											C_{X1}	C_{X2}	V_{CX} +2.0 V	V_{EE} -3.2 V	V_{CC} +2.0 V
Rise Time (10% to 90%)	t_+	6	–	3.6	–	–	3.5	–	3.8	ns	–	11,14	2	8	1,5
Fall Time (10% to 90%)	t_-	6	–	3.1	–	–	3.0	–	3.3	ns	–	11,14	2	8	1,5
Oscillator Frequency	f_{osc1}	–	130	–	130	155	190	110	–	MHz	–	11,14	2	8	1,5
	f_{osc2}	–	–	–	78	90	120	–	–	MHz	11,14	–	2	8	1,5
Tuning Ratio Test †	TR	–	–	–	3.1	4.5	–	–	–	–	11,14	–	–	8	1,5

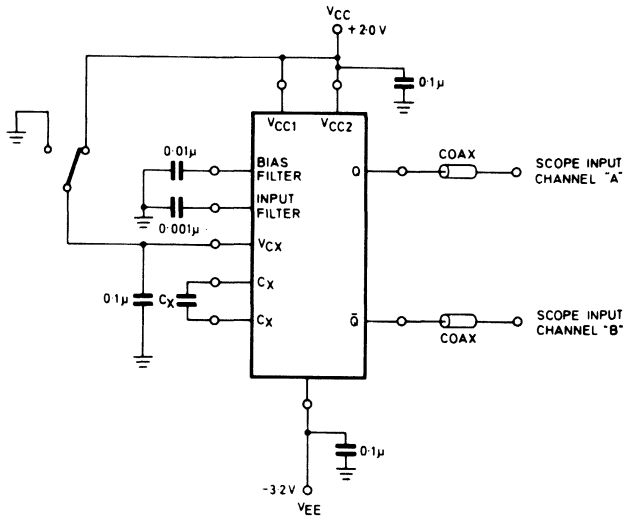
*Germanium diode (0.4 drop) forward biased from 11 to 14 (11 ——▶|—— 14)

**Germanium diode (0.4 drop) forward biased from 14 to 11 (11 ——|◀—— 14)

†$TR = \frac{\text{Output frequency at } V_{CX} = +2.0\text{ V}}{\text{Output frequency at } V_{CX} = \text{Gnd}}$

CX1 = 10pF connected from pin 11 to pin 14

CX2 = 5pF connected from pin 11 to pin 14



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $<\frac{1}{4}$ inch from TP_{in} to input pin and TP_{out} to output pin.

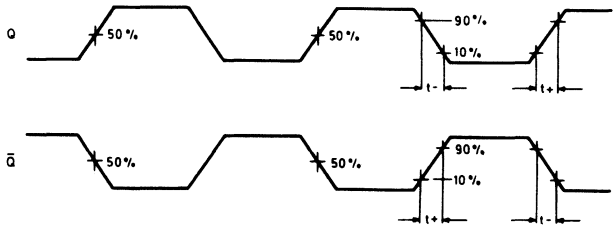


Fig. 3 Switching time test circuit and waveforms

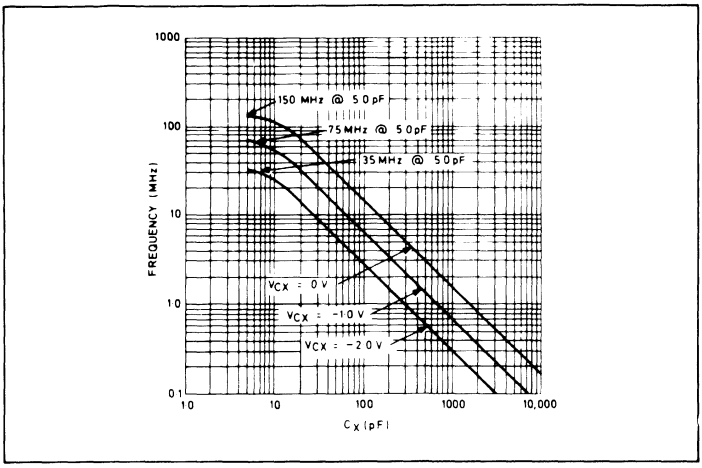


Fig.4 Output frequency v capacitance for three values of input voltage

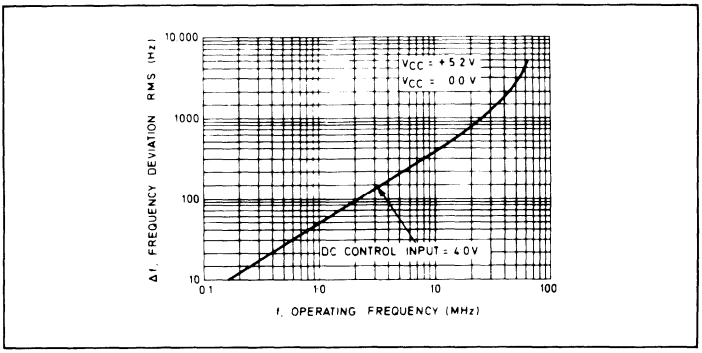


Fig.5 RMS noise deviation v operating frequency

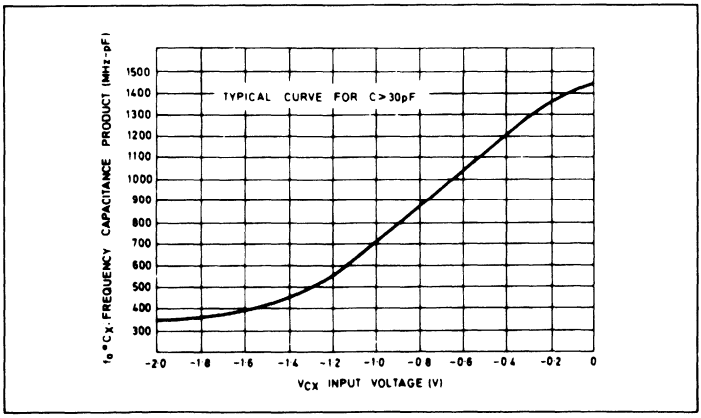


Fig.6 Frequency-capacitance product v control voltage V_{CX}

PLESSEY
Semiconductors

SP1660

DUAL 4-INPUT OR/NOR GATE

SP1660 provides simultaneous OR-NOR output functions with the capability of driving 50Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (-30°C to +85°C). The input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

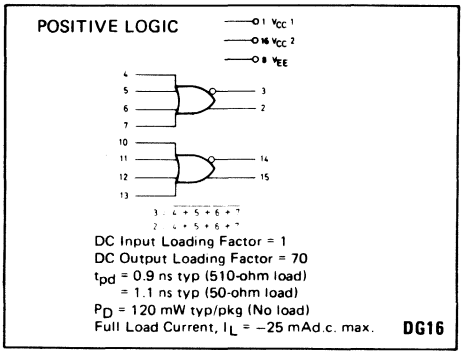


Fig. 1 Logic diagram

FEATURES

- Gate Switching Speed Ins Typ.
- ECL 10000- Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

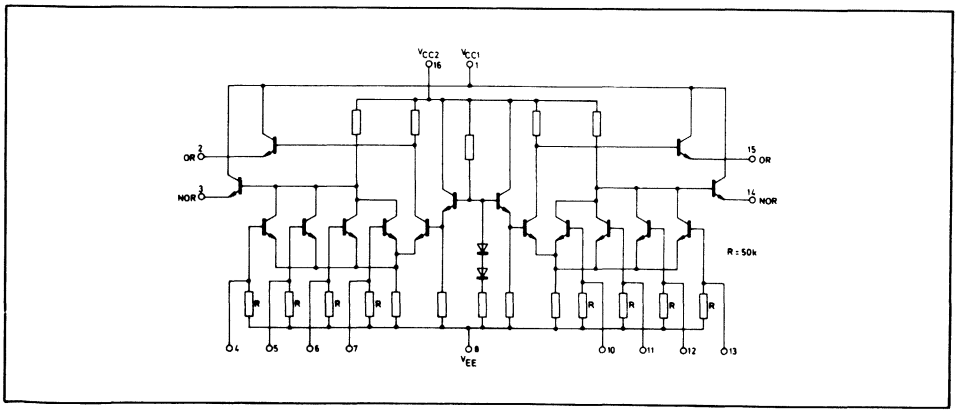


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested with a 50-ohm resistor to −2.0 Vdc.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1660 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
NOR Logic "1" Output Voltage	V_{OH}	3	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic "0" Output Voltage	V_{OL}	3	-1.890	1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic "1" Threshold Voltage	V_{OHA}	3	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	4	8	1,16
				–		–		–		–	–	–	5		
				–		–		–		–	–	–	6		
				–		–		–		–	–	–	7		
NOR Logic "0" Threshold Voltage	V_{OLA}	3	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	4	–	8	1,16
			–		–		–			–	–	5	–		
			–		–		–			–	–	6	–		
			–		–		–			–	–	7	–		
OR Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	4	–	8	1,16
				–		–		–		–	–	5	–		
				–		–		–		–	–	6	–		
				–		–		–		–	–	7	–		
OR Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	4	8	1,16
			–		–		–			–	–	–	5		
			–		–		–			–	–	–	6		
			–		–		–			–	–	–	7		
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3		1.8	–	1.7	–	1.9	ns	4	3	–	–	8	1,16
	t_{4-2-}	2		1.8	–	1.7	–	1.9			2	–	–		
	t_{4+2+}	2		1.6	–	1.5	–	1.7			2	–	–		
	t_{4-3+}	3	–	1.6	–	1.5	–	1.7			3	–	–		
Rise Time	t_{3+}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{3-}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to the input under test.

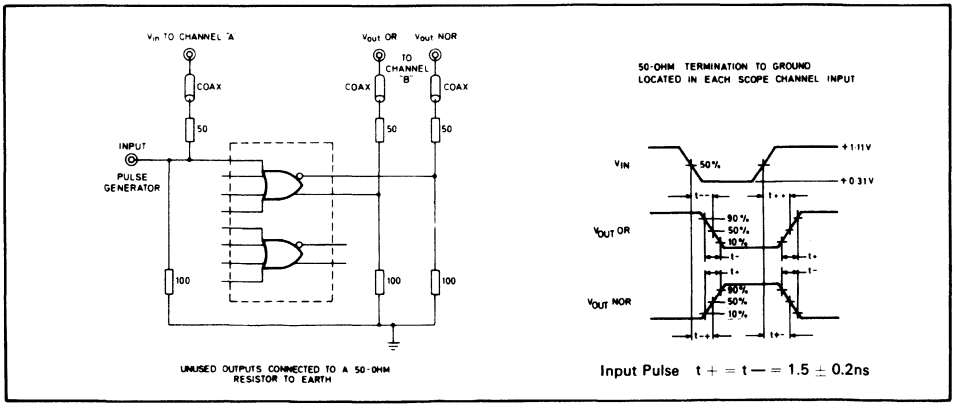


Fig. 3 Switching time test circuit and wave forms at +25°C

PLESSEY
Semiconductors

SP1670

MASTER/SLAVE TYPE D FLIP-FLOP

The SP1670 is a D-type Master-Slave Flip-Flop designed for use in high speed digital applications. Master-slave construction renders the SP1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

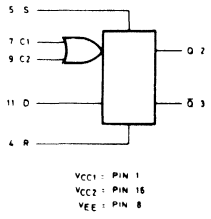
When both clock inputs (C1 and C2) are in the low state, the data input affects only the Master portion of the flip-flop. The data present in the Master is transferred to the Slave when clock inputs (C1 OR C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 OR C2 is in the high state the Master (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



DC Input Loading Factor = C1, C2 = 0.67 D = 0.75 R,S = 1.5
DC Output Loading Factor = 70
Power Dissipation = 220 mW typical (No Load)
f_{tog} = 350 MHz typ **DG16**

Fig. 1 Logic diagram

FEATURES

- Toggle Frequency > 300 MHz
- ECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

TRUTH TABLE				
R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	↑	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	↑	H
L	L	H	H	Q_n

ϕ = Don't Care
ND = Not Defined
C = C1 + C2

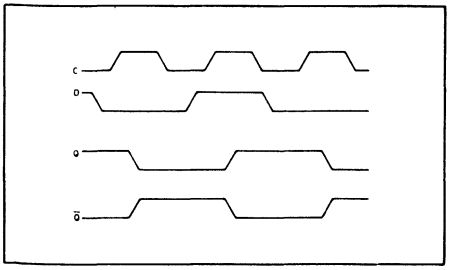


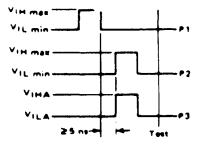
Fig. 2 Timing diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the d.c. specifications shown in the characteristics table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained. Outputs are terminated through a 50Ω resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1670 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	-85°C Min	-85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P_1	P_2	P_3	(V_{CC}) Gnd
Power Supply Drain	I_E	8	–	–	–	48	–	–	mAdc	7,9	–	–	–	8	–	–	–	1,16
Input Current	$I_{in\ H}$	4	–	–	–	550	–	–	μAdc	4	–	–	–	8	–	–	–	1,16
		5	–	–	–	550	–	–		5	–	–	–		–	–	–	
		9	–	–	–	250	–	–		9	–	–	–		–	–	–	
		7	–	–	–	250	–	–		7	–	–	–		–	–	–	
		11	–	–	–	270	–	–		11	–	–	–		–	–	–	
	$I_{in\ L}$	4	–	–	0.5	–	–	–	μAdc	9	4	–	–	8	–	–	–	1,16
		5	–	–		–	–	–		9	5	–	–		–	–	–	
		9	–	–		–	–	–		7	9	–	–		–	–	–	
		7	–	–		–	–	–		9	7	–	–		–	–	–	
		11	–	–		–	–	–		9	11	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	4,7,11	–	–	8	9	5	–	1,16
		3								11	5,9	–	–		7	4	–	
		2								11	5,7	–	–		4	9	–	
		3								–	4,9,11	–	–		5	7	–	
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	11	5,7	–	–	8	9	4	–	1,16
		3								–	4,9,11	–	–		7	5	–	
		2								–	4,7,11	–	–		5	9	–	
		3								11	5,9	–	–		4	7	–	
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	4,7,11	–	–	8	9	–	5	1,16
		3		–		–		–		11	5,9	–	–		7	–	4	
		2		–		–		–		11	5,7	–	–		4	–	9	
		3		–		–		–		–	4,9,11	–	–		5	–	7	
		2		–		–		–		–	5,7	11	–		4	9	–	
		3		–		–		–		–	4,9	–	11		5	7	–	
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	1.600	–	1.555	Vdc	11	5,7	–	–	8	9	–	4	1,16
		3	–		–		–			–	4,9,11	–	–		7	–	5	
		2	–		–		–			–	4,7,11	–	–		5	–	9	
		3	–		–		–			11	5,9	–	–		4	–	7	
		2	–		–		–			–	4,7	–	11		5	9	–	
		3	–		–		–			–	5,9	11	–		4	7	–	
Switching Parameters			Min	Max	Min	Max	Min	Max						-3.2 Vdc				+2.0 Vdc
Clock to Output Delay (See Figure 1)	t_{9+2+}	9,2	1.0	2.7	1.1	2.5	1.1	2.9	ns	–	–	–	–	8	–	–	–	1,16
	t_{9+2-}	9,2								–	–	–	–		–	–	–	
	t_{9+3+}	9,3								–	–	–	–		–	–	–	
	t_{9+3-}	9,3								–	–	–	–		–	–	–	
Set to Output Delay (See Figure 2)	t_{5+2+}	5,2								–	–	–	–		–	–	–	
	t_{5+3-}	5,3								–	–	–	–		–	–	–	
Reset to Output Delay (See Figure 2)	t_{4+2-}	4,2								–	–	–	–		–	–	–	
	t_{4+3+}	4,3								–	–	–	–		–	–	–	
Output Rise Time	$t_{2+/3+}$	2,3	0.9	2.7	1.0	2.5	1.0	2.9		–	–	–	–		–	–	–	
Fall Time (See Figure 2)	$t_{2-/3-}$	2,3	0.5	2.1	0.6	1.9	0.6	2.3		–	–	–	–		–	–	–	
Set Up Time (See Figure 3)	$t_{1/1}$	2	–	–	–	0.4	–	–		–	–	–	–		–	–	–	
	$t_{1/0}$	2	–	–	–	0.5	–	–		–	–	–	–		–	–	–	
Hold Time (See Figure 3)	$t_{H/1}$	2	–	–	–	0.3	–	–		–	–	–	–		–	–	–	
	$t_{H/0}$	2	–	–	–	0.5	–	–		–	–	–	–		–	–	–	
Toggle Frequency (See Figure 4)	f_{Tog}	2	270	–	300	–	270	–	MHz	–	–	–	–		–	–	–	–



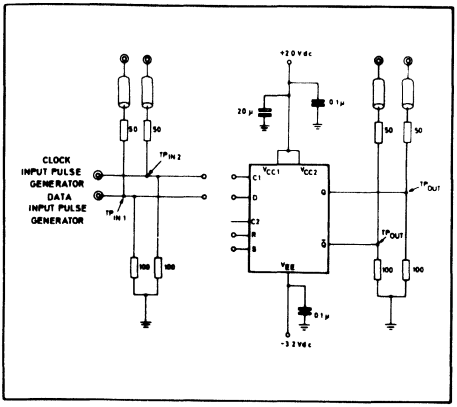


Fig. 3 Propagation delay test circuit

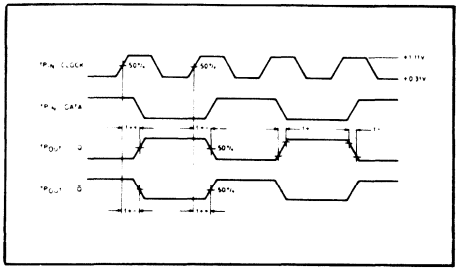


Fig. 4 Clock delay waveforms at +25°C

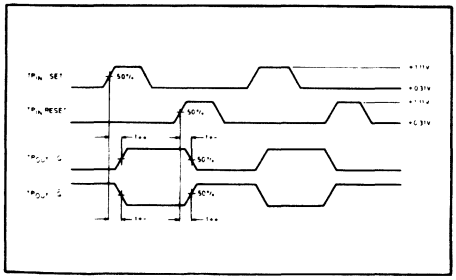


Fig. 5 Set/reset delay waveform at +25°C

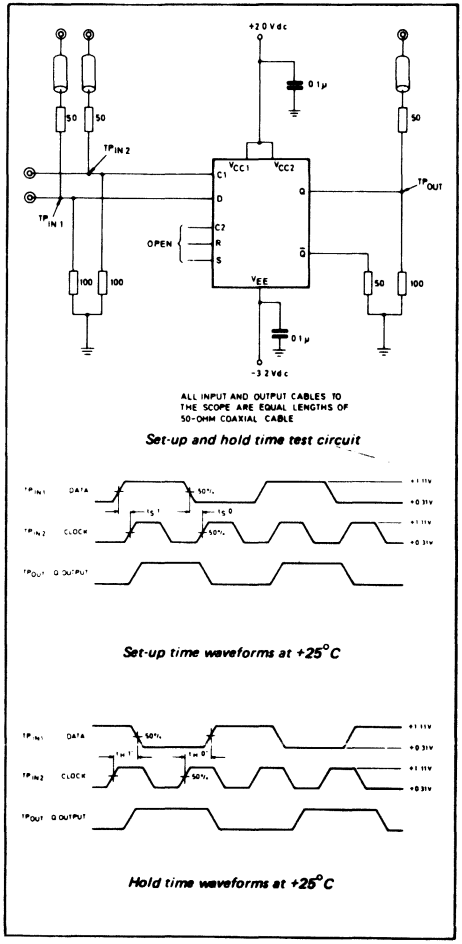


Fig. 6 Set-up and hold time test circuit

Set up time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock (C) that information must remain unchanged at the data (D) input.

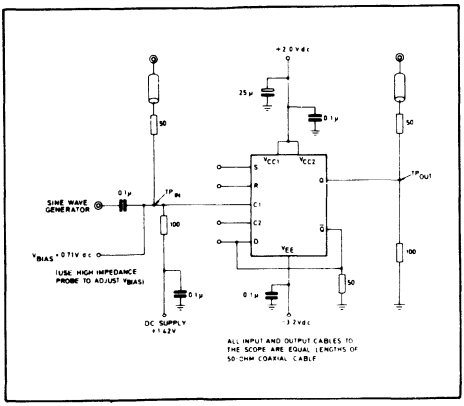


Fig. 7 Toggle frequency test circuit

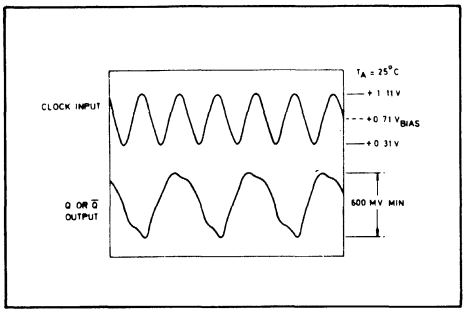


Fig. 8 Toggle frequency waveforms

The maximum toggle frequency of the SP1670 has been exceeded when either:
1. The output peak-to-peak voltage swing falls below 600mV
OR
2. The device ceases to toggle (divide by two). V_{Bias} is defined by the test circuit Fig. 7 and by the waveform in Fig. 8.

Temperature	−30°C	+25°C	+85°C
V_{Bias}	+0.660V	+0.710V	+0.765V

Table 1 Variation of V_{Bias} with temperature

Figures 9 and 10 illustrate minimum clock pulse width recommended for reliable operation of the SP1670

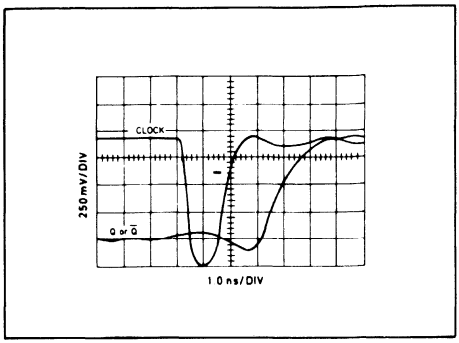


Fig. 9 Minimum 'down time' to clock (Output load = 50Ω)

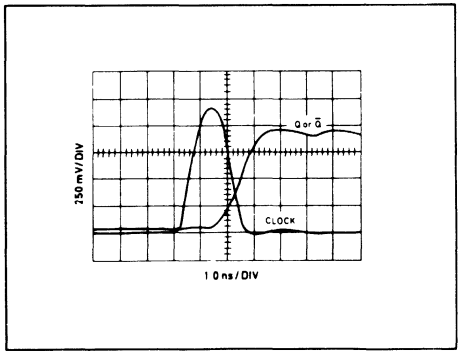


Fig. 10 Minimum 'up time' to clock (Output load = 50Ω)

Operation of the Master-Slave Type D Flip-Flop

In the circuit of Figure 11 assume that initially Q, C, R, S and D are at 0 levels and that $\overline{Q}$ is at the 1 level. Since the clock is low, transistors TR3 and TR22 are conducting. In the slave section only transistors TR25 and TR26 are in series with TR22. The output of the slave section is fed back to these two transistors in order to form a latch. Thus, when the clock is low, the output state of the slave is maintained. In the master section, the current path is through TR3 and TR9.

Now assume that the data input goes high. The high-input signal on the base of TR4 causes it to conduct, and TR9 to turn off. The voltage drop across resistor RC1 causes a low-state voltage on the base and therefore on the emitter of TR11. Since there is essentially no current flow through RC2, the base of transistor TR10 is in a high state. This is reflected in the emitter, and in turn is transferred to the base of TR6. TR6 is biased for conduction but, since there is no current path, does not conduct.

Now allow the clock to go high. As the clock signal rises, transistor TR2 turns on and transistor TR3 turns off. This provides a current path for the common-emitter transistors TR5, TR6, TR7, and TR8. Since the bases of all these devices except TR6 are in the low state, current flow is through TR6. This maintains the base and emitter of TR11 low, and the base and emitter of TR10 high. The high state on TR10 is transferred to TR23 of the slave section. As the clock continues to rise TR21 begins to turn on and TR22 to turn off. (Reference voltages in the master and slave units are slightly offset to ensure prior clocking of the master section.) With transistor TR21 conducting and the base of TR23 in a high state, the current path now includes TR21, TR23, and resistor RC3. The voltage drop across the resistor places a low state voltage on the base, and therefore the emitter, of TR30. The lack of current flow through RC4 causes a high state input to the base of TR29. These states are fed back to the latch transistors, TR25 and TR26.

As the clock voltage falls, transistor TR21 turns off and TR22 turns on. This provides a current path through the latch transistors, locking-in the slave output.

In the master section the falling clock voltage turns on transistor TR3 and turns off TR2. This enables the input transistor TR4 so that the master section will again track the D input.

The separation of thresholds between the master and slave flip-flops is caused by R8. The current through this resistor produces an offset between the thresholds of the transistor pairs TR2:TR3 and TR21:TR22. This offset disables the D input of the master flip-flop prior to the enabling of the information transfer from master to slave via transistors TR23 and TR28. This disabling operation prevents false information from being transferred directly from master to slave during the clock transition, particularly if the D input changes at this time (such as in a counting operation where the $\overline{Q}$ output is tied back to D). The offsetting resistor also allows a relatively slow-rising clock waveform to be used without the danger of losing information during the transition of the clock.

The set and reset inputs are symmetrically connected. Therefore, their action is similar although results are opposite. As a logic 1 level is applied to the S input transistor, TR2 begins to conduct because its base is now being driven through TR19 which is in turn connected to S. Transistor TR5 is now on and the feedback devices TR6 and TR7 latch this information into the master flip-flop. A similar action takes place in the slave with transistors TR21, TR24, TR25, and TR26.

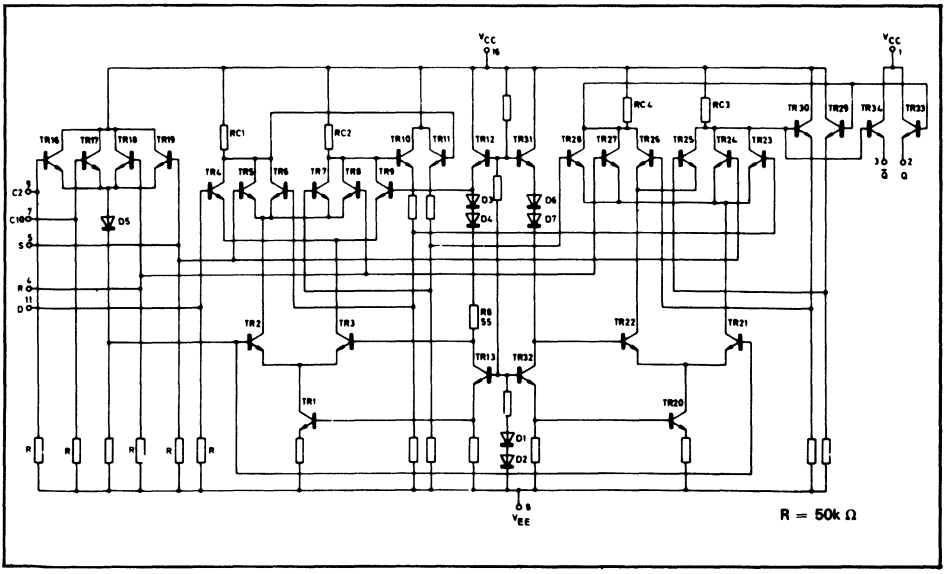


Fig. 11 SP1670 Circuit diagram

PLESSEY
Semiconductors

SP16F60

DUAL 4-INPUT OR/NOR GATE

SP16F60 provides simultaneous OR-NOR output functions with the capability of driving 50 Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (−30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

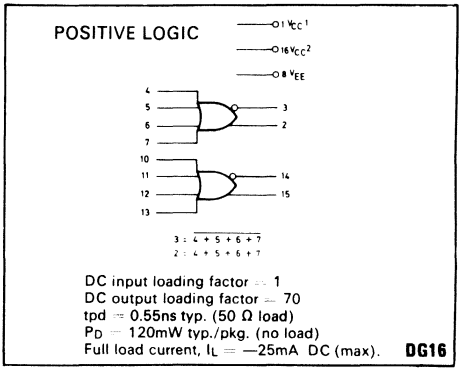


Fig. 1 Logic diagram

FEATURES

- Gate Switching Speed 550ps Typ.
- ECL III and ECL 10K Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation
- Pin and Power Compatible with SP1660

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems
- Nucleonics

ABSOLUTE MAXIMUM RATINGS

Power supply voltage | V_{CC} - V_{EE} |	8V
Base input voltage	0V to V_{EE}
O/P source current	<40mA
Storage temperature	−55°C to +150°C
Junction operating temperature	< +125C

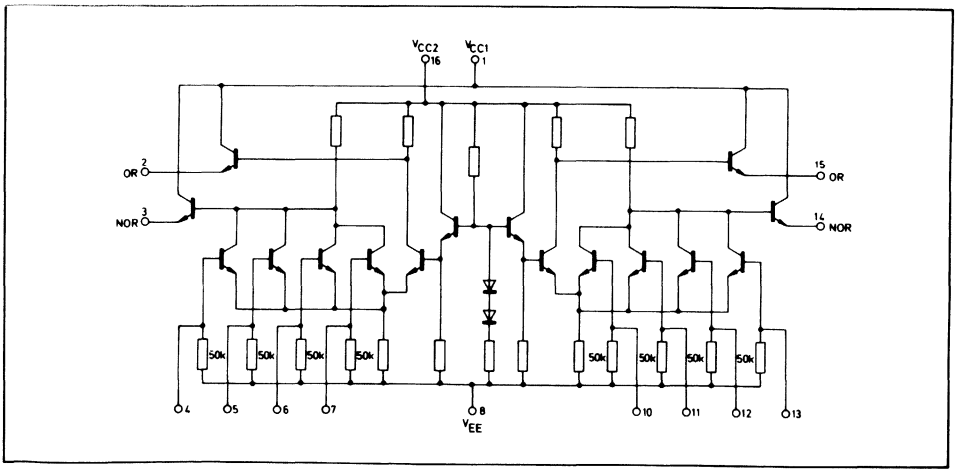


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

@ Test Temperature	TEST VOLTAGE VALUES (V) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP16F60 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Units	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mA	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μA	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μA	–	*	–	–	8	1,16
NOR Logic 1 Output Voltage	V_{OH}	3	-1.045	-0.875	-0.960	-0.810	-1.890	-0.700	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 0 Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 1 Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 0 Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 1 Threshold Voltage	V_{OHA}	3	-1.065	–	-0.980	–	-0.910	–	V	–	–	–	4	8	1,16
			–	–	–	–	–	–		–	–	–	5		
			–	–	–	–	–	–		–	–	–	6		
			–	–	–	–	–	–		–	–	–	7		
NOR Logic 0 Threshold Voltage	V_{OLA}	3	–	-1.630	–	-1.600	–	-1.555	V	–	–	4	–	8	1,16
			–	–	–	–	–	–		–	–	5	–		
			–	–	–	–	–	–		–	–	6	–		
			–	–	–	–	–	–		–	–	7	–		
OR Logic 1 Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	V	–	–	4	–	8	1,16
			–	–	–	–	–	–		–	–	5	–		
			–	–	–	–	–	–		–	–	6	–		
			–	–	–	–	–	–		–	–	7	–		
OR Logic 0 Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	V	–	–	–	4	8	1,16
			–	–	–	–	–	–		–	–	–	5		
			–	–	–	–	–	–		–	–	–	6		
			–	–	–	–	–	–		–	–	–	7		
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out			-3.2V	+2.0V
Propagation Delay	t_{4+3-}	3	–	–	0.55	0.8	–	–	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	–	–			–	–			2	–	–		
	t_{4+2+}	2	–	–			–	–			2	–	–		
	t_{4-3+}	3	–	–			–	–			3	–	–		
Rise Time 20% to 80%	t_{3+}	3			0.4	0.6			ns	4	3	–	–	8	1,16
	t_{2+}	2			0.35	0.6	–	–	ns	4	2	–	–	8	1,16
Fall Time 20% to 80%	t_{3-}	3			0.4	0.6	–	–	ns	4	3	–	–	8	1,16
	t_{2-}	2			0.35	0.6	–	–	ns	4	2	–	–	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to the input under test

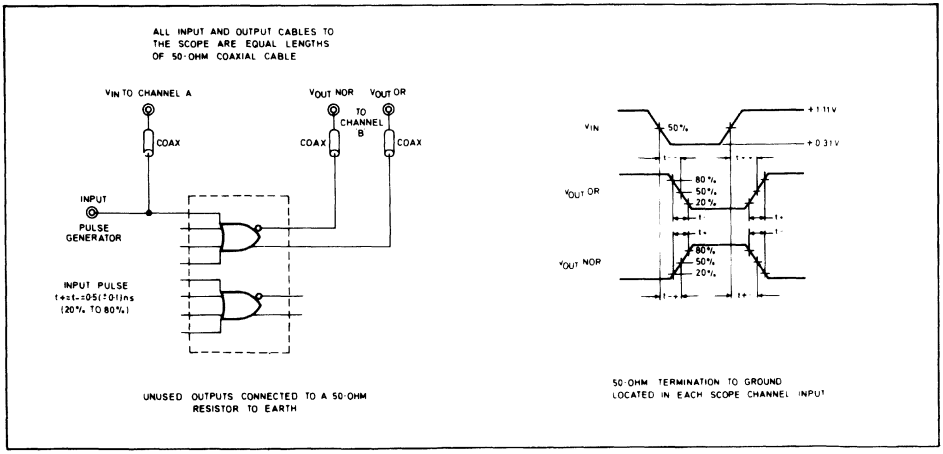


Fig. 3 Switching time test circuit and waveforms at +25 C

PLESSEY
Semiconductors

SP16F70

MASTER/SLAVE D TYPE FLIP-FLOP

The SP16F70 is a D-type Master-Slave Flip-Flop designed for use in high speed digital applications. Master-slave construction renders the SP16F70 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the Master portion of the flip-flop. The data present in the Master is transferred to the Slave when clock inputs (C1 OR C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 OR C2 is in the high state the Master (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}

FEATURES

- Toggle Frequency >350MHz
- ECL 10000 Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

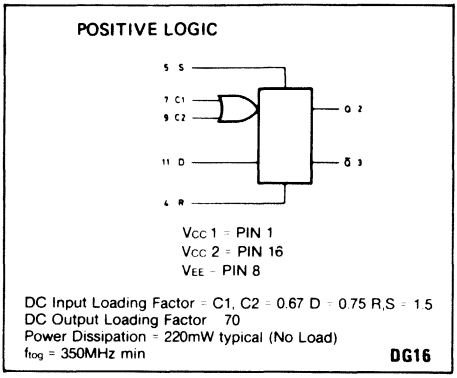


Fig. 1 Logic diagram

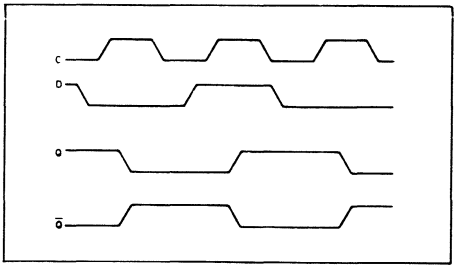


Fig. 2 Timing diagram

TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	↓	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	↓	H
L	L	H	H	Q_n

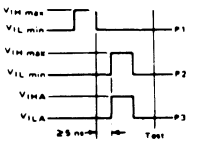
ϕ = Don't Care
ND = Not Defined
C = C1 + C2

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the d.c. specifications shown in the characteristics table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained. Outputs are terminated through a 50Ω resistor to −2.0 volts.

Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P_1	P_2	P_3	(V_{CC}) Gnd
Power Supply Drain	I_E	8	–	–	–	48	–	–	mAdc	7,9	–	–	–	8	–	–	–	1,16
Input Current	I_{inH}	4	–	–	–	550	–	–	μAdc	4	–	–	–	8	–	–	–	1,16
		5	–	–	–	550	–	–		5	–	–	–		–	–	–	
		9	–	–	–	250	–	–		9	–	–	–		–	–	–	
		7	–	–	–	250	–	–		7	–	–	–		–	–	–	
		11	–	–	–	270	–	–		11	–	–	–		–	–	–	
	I_{inL}	4	–	–	0.5	–	–	–	μAdc	9	4	–	–	8	–	–	–	1,16
		5	–	–		–	–	–		9	5	–	–		–	–	–	
		9	–	–		–	–	–		7	9	–	–		–	–	–	
		7	–	–		–	–	–		9	7	–	–		–	–	–	
		11	–	–		–	–	–		9	11	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	4,7,11	–	–	8	9	5	–	1,16
		3								11	5,9	–	–		7	4	–	
		2								11	5,7	–	–		4	9	–	
		3								–	4,9,11	–	–		5	7	–	
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	11	5,7	–	–	8	9	4	–	1,16
		3								–	4,9,11	–	–		7	5	–	
		2								–	4,7,11	–	–		5	9	–	
		3								11	5,9	–	–		4	7	–	
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	4,7,11	–	–	8	9	–	5	1,16
		3		–		–		–		11	5,9	–	–		7	–	4	
		2		–		–		–		11	5,7	–	–		4	–	9	
		3		–		–		–		–	4,9,11	–	–		5	–	7	
		2		–		–		–		–	5,7	11	–		4	9	–	
		3		–		–		–		–	4,9	–	11		5	7	–	
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	11	5,7	–	–	8	9	–	4	1,16
		3	–		–		–			–	4,9,11	–	–		7	–	5	
		2	–		–		–			–	4,7,11	–	–		5	–	9	
		3	–		–		–			11	5,9	–	–		4	–	7	
		2	–		–		–			–	4,7	–	11		5	9	–	
		3	–		–		–			–	5,9	11	–		4	7	–	
Switching Parameters			Min	Max	Min	Max	Min	Max						-3.2 Vdc				+2.0 Vdc
Clock to Output Delay	t9+2+	9,2	1.0	2.7	1.1	2.5	1.1	2.9	ns	–	–	–	–	8	–	–	–	1,16
	t9+2−	9,2								–	–	–	–		–	–	–	
	t9+3+	9,3								–	–	–	–		–	–	–	
	t9+3−	9,3								–	–	–	–		–	–	–	
Set to Output Delay	t5+2+	5,2								–	–	–	–		–	–	–	
	t5+3−	5,3								–	–	–	–		–	–	–	
Reset to Output Delay	t4+2−	4,2								–	–	–	–		–	–	–	
	t4+3+	4,3								–	–	–	–		–	–	–	
Output Rise Time	t_{r2-13+}	2,3	0.9	2.7	1.0	2.5	1.0	2.9		–	–	–	–		–	–	–	
Fall Time	t_{f2-13-}	2,3	0.5	2.1	0.6	1.9	0.6	2.3		–	–	–	–		–	–	–	
Set Up Time	t_s"1"	2	–	–	–	0.4	–	–		–	6	–	–		–	–	–	
	t_s"0"	2	–	–	–	0.5	–	–		–	6	–	–		–	–	–	
Hold Time	t_H"1"	2	–	–	–	0.3	–	–		–	6	–	–		–	–	–	
	t_H"0"	2	–	–	–	0.5	–	–		–	6	–	–		–	–	–	
Toggle Frequency	f_{Tog}	2	350	–	350	–	350	–	MHz	–	–	–	–		–	–	–	–



PLESSEY
Semiconductors

JUL 82
ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

SP9131

520MHz ECL DUAL D FLIP-FLOP

The SP9131 Dual D type flip-flop is pin compatible with 10131, but has improved dynamic performance.

FEATURES

- Guaranteed Operation at 520MHz
- Separae or Common Clock
- Independent Set and Reset Inputs
- Master Slave Operation
- -5.2V Supply
- Operating Temperature Range -30°C to +85°C
- ECL 10K Compatible
- Pin Compatible with MC10131

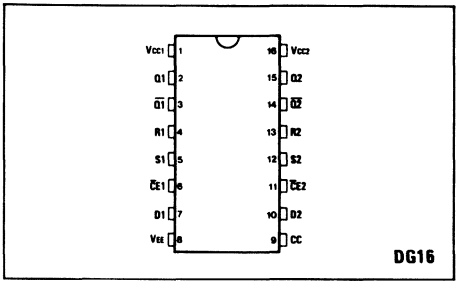


Fig.1 Pin connections - top view

R-S TRUTH TABLE

R	S	Qn + 1
L	L	Qn
L	H	H
H	L	L
H	H	ND

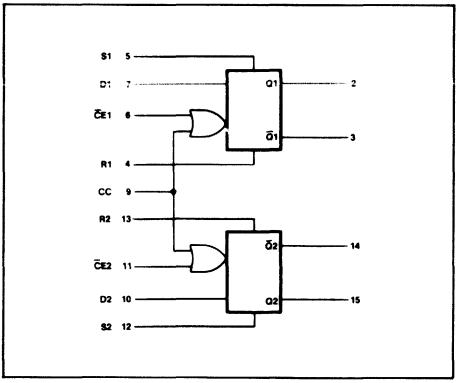


Fig.2 SP9131 logic diagram

CLOCKED TRUTH TABLE

C	D	Qn + 1
L	X	Qn
H	L	L
H	H	H

X = Don't care
C = CE + CC
A clock H is a clock transition from a low to a high state.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	| VCC - VEE | 8V
Base input voltage	0V to VEE
Output source current	<40mA
Storage temperature	-55°C to +150°C
Junction operating temperature	< +125°C

ELECTRICAL CHARACTERISTICS

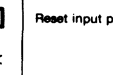
The SP9131 circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to -2 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

Test temp.	TEST VOLTAGES (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}
-30° C	-0.89	-1.89	-1.205	-1.500	-5.2
+25° C	-0.81	-1.85	-1.105	-1.475	-5.2
+85° C	-0.70	-1.825	-1.035	-1.440	-5.2

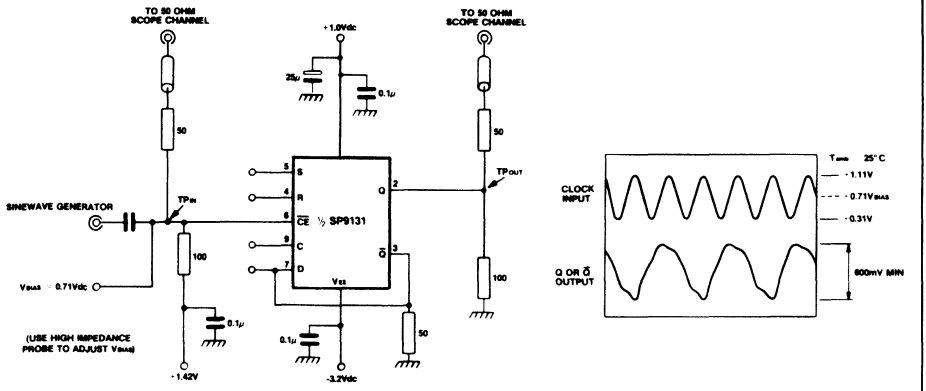
Characteristic	Symbol	Pin under test	Test limits -30° C Min.	-30° C Max.	+25° C Min.	+25° C Typ.	+25° C Max.	+85° C Min.	+85° C Max.	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}	V_{CC} (GND)
Power supply current	I_E	8	-	95	-	70	87	-	95	mA	-	-	-	-	8	1.16
Input current	I_{inH}	4	-	-	-	-	600	-	-	µA	4	-	-	-	8	1.16
		5	-	-	-	-	600	-	-		5	-	-	-		
		6	-	-	-		300	-	-		6	-	-	-		
		7	-	-	-	-	300	-	-		7	-	-	-		
		9	-	-	-	-	420	-	-		9	-	-	-		
Input leakage current	I_{inL}	4,5 (Note 1)	-	-	0.5	-	-	-	-	µA	-	-	-	-	8	1.16
		6,7,9 (Note 1)	-	-	0.5	-	-	-	-	µA	-	-	-	-	8	1.16
Logic '1' output voltage	V_{OH}	2	-1.06	-0.89	-0.96	-	-0.81	-0.89	-0.70	V	5	-	-	-	8	1.16
		2 (Note 2)	-1.06	-0.89	-0.96	-	0.81	-0.89	-0.70	V	7	-	-	-	8	1.16
Logic '0' output voltage	V_{OL}	3	-1.89	-1.675	-1.85	-	-1.65	-1.825	-1.615	V	5	-	-	-	8	1.16
		3 (Note 2)	-1.89	-1.675	-1.85	-	-1.65	-1.825	-1.615	V	7	-	-	-	8	1.16
Logic '1' threshold voltage	V_{OHA}	2	-1.08	-	-0.98	-	-	-0.91	-	V	-	-	5	-	8	1.16
		2 (Note 2)	-1.08	-	-0.98	-	-	-0.91	-	V	-	-	7	9	8	1.16
Logic '0' threshold voltage	V_{OLA}	3	-	-1.655	-	-	-1.63	-	-1.595	V	-	-	5	-	8	1.16
		3 (Note 2)	-	-1.655	-	-	-1.63	-	-1.595	V	-	-	7	9	8	1.16
SWITCHING TIMES											**+1.11V**		**Pulse in**	**Pulse out**	**-3.2V**	**+2.0V**
Clock input propagation delay	t_{9+2-}	2	0.5	1.8	0.5	1.0	1.8	0.6	2.1	ns	-	-	9	2	8	1.16
	t_{9+2+}	2	-	-				-	-		7	-	9	2		
	t_{8+2+}	2	-	-				-	-		7	-	6	2		
	t_{8+2-}	2	-	-				-	-		-	-	6	2		
Rise time (20 to 80 %)	t_{2+}	2	0.5	1.5	0.5	1.0	1.5	0.5	1.6		7	-	9	2		
Fall time (20 to 80 %)	t_{2-}	2	0.4	1.4	0.4		1.4	0.5	1.5		-	-	9	2		
Set input propagation delay	t_{5+2+}	2	0.5	2.0	0.5	1.0	2.0	0.6	2.3	ns	-	-	5	2	8	1.16
	t_{12+15+}	15	-	-				-	-		6	-	12	15		
	t_{5+3-}	3	-	-				-	-		-	-	5	3		
	t_{12+14-}	14	-	-				-	-		9	-	12	14		
Reset input propagation delay	t_{4+2-}	2	-	-		1.0		-	-	ns	-	-	4	2	8	1.16
	t_{13+15-}	15	-	-				-	-		6	-	13	15		
	t_{4+3-}	3	-	-				-	-		-	-	4	3		
	t_{13+14+}	14	-	-				-	-		9	-	13	14		
Setup time	t_{setup}	7	1.0	-	1.0	-		1.0	-	ns	-	-	6.7	2	8	1.16
Hold time	t_{hold}	7	0.2	-	0.2	-		0.2	-	ns	-	-	6.7	2	8	1.16
Toggle frequency (max.)	f_{Tog}	2	520	-	520	600	-	500	-	MHz	-	-	6	2	8	1.16

NOTES

1. Individually test each input, apply V_{IL} min to pin under test.
2. Output level to be measured after a clock pulse has been applied to the CE input (pin 6).



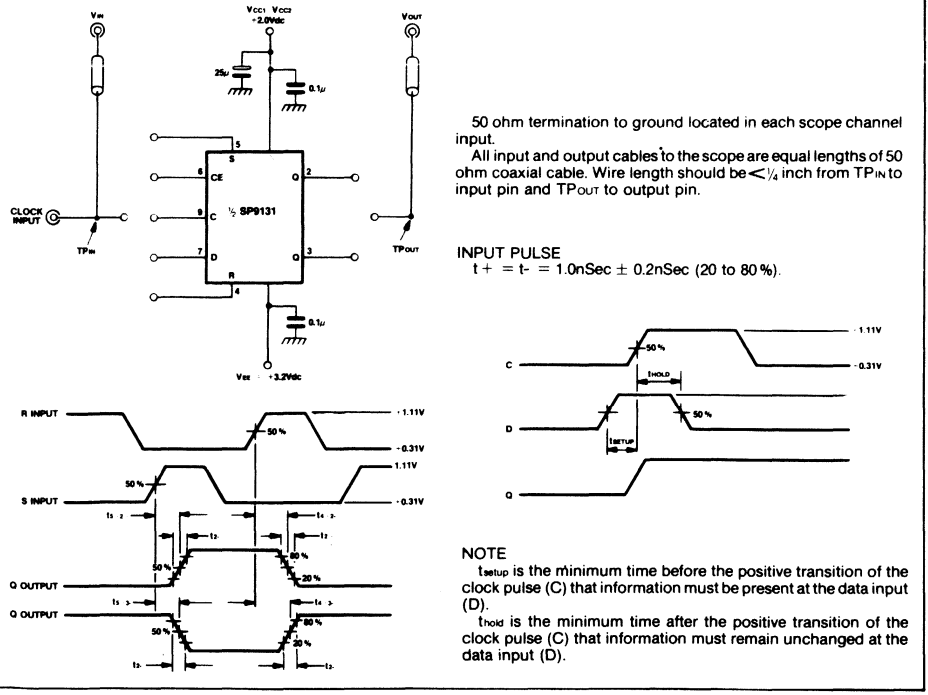
TEST CIRCUIT DETAILS



50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be $<1/4$ inch from TP_{IN} to input pin and TP_{OUT} to output pin.

Fig.3 Toggle frequency test circuit



50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be $<1/4$ inch from TP_{IN} to input pin and TP_{OUT} to output pin.

INPUT PULSE

$t+ = t- = 1.0nSec \pm 0.2nSec$ (20 to 80 %).

NOTE

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

Fig.4 Switching time test circuit and waveforms at 25° C

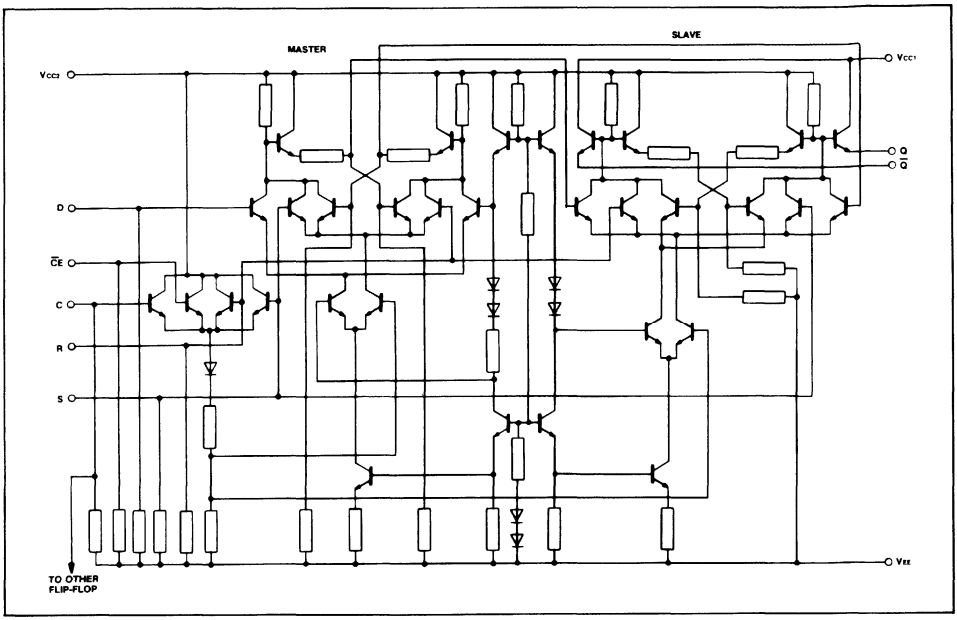


Fig.5 Circuit schematic (½ of circuit shown)

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SP9210

200MHz 8-BIT LATCH

The SP9210 is a dual 4-bit master/slave D-type flip-flop with asynchronous set and reset which override the clock input.

Data is entered into the master when the clock is low and is transferred to the slave on the positive transition of the clock, the device being edge-sensitive.

On-chip pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

FEATURES

- Dual 4-Bit Master/Slave D-Type Flip-Flop
- Clock Rate in Excess of 200MHz
- -5.2V Supply
- Current Consumption Typically 145mA
- Input Current Less Than 330µA
- Operating Temperature Range -30°C to +85°C
- Set and Reset Inputs Provided
- ECL 10K Compatible
- Dual Clock Inputs

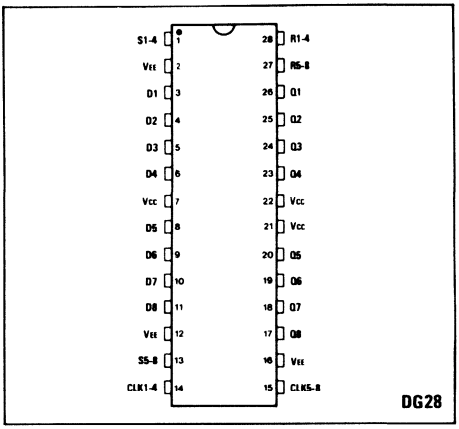


Fig.1 Pin connections - top view

PIN NAMES

S1-4	Set input for 1-4
S5-8	Set input for 5-8
V_{EE}	Supply voltage (-VE)
D1-8	Data inputs 1-8
CLK1-4	Clock latch for 1-4
CLK5-8	Clock latch for 5-8
Q1-8	Outputs latches 1-8
R1-4	Reset input latch for 1-4
R5-8	Reset input latch for 5-8

R - S TRUTH TABLE

R	S	Qn + 1
L	L	Qn
L	H	H
H	L	L
H	H	ND

R = Reset, S = Set,
ND = Not defined

CLOCKED TRUTH TABLE

C	D	Qn + 1
L	X	Qn
↑	L	L
↑	H	H

C = Clock, D = Data,
↑ = Rising edge, X = Don't care

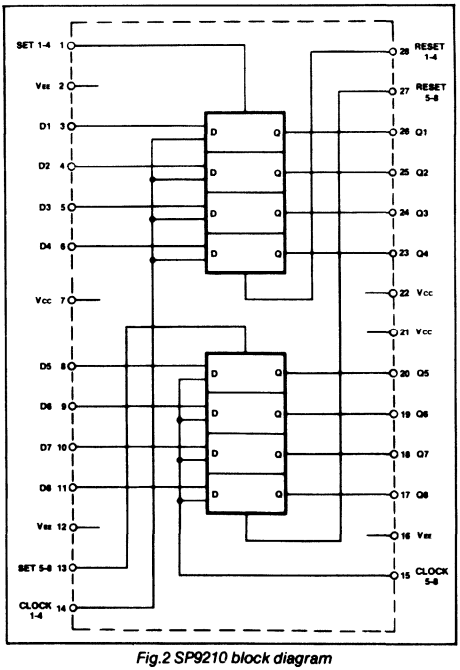


Fig.2 SP9210 block diagram

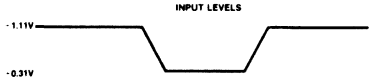
ELECTRICAL CHARACTERISTICS

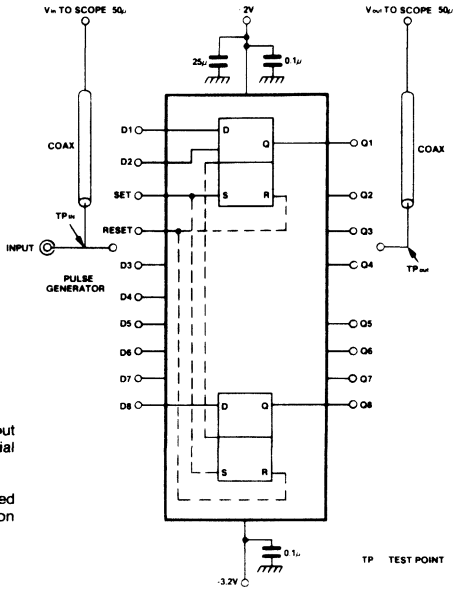
Each circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to -2 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

Test temp.	TEST VOLTAGES (V) V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}
-30° C	-0.89	-1.89	-1.205	-1.500	-5.2
+25° C	-0.810	-1.850	-1.105	-1.475	-5.2
+85° C	-0.70	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin under test	-30° C Min.	-30° C Max.	+25° C Min.	+25° C Typ.	+25° C Max.	+85° C Min.	+85° C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX.	V_{IL} MIN.	V_{IHA} MIN.	V_{ILA} MAX.	V_{EE}	V_{CC} (GND)
POWER SUPPLY																
Drain current	I_{EE}	2,12,16	-	200	-	145	180	-	200	mA	-	-	-	-	2,12,16	7,21,22
Input current	I_{INH}	Set/Reset	-	-	-	-	330	-	-	µA	Note 1	-	-	-	2,12,16	7,21,22
		Clock	-	-	-	-	330	-	-	µA	Note 1	-	-	-	2,12,16	7,21,22
		Data	-	-	-	-	330	-	-	µA	Note 1	-	-	-	2,12,16	7,21,22
Input leakage current	I_{INL}	All inputs	-	-	0.5	-	-	-	-	µA	-	Note 1	-	-	2,12,16	7,21,22
Logic '1' output voltage	V_{OH}	All outputs (Note 2)	-1.06	-0.89	-0.96	-	-0.81	-0.89	-0.70	V	Data inputs	-	-	-	2,12,16	7,21,22
Logic '0' output voltage	V_{OL}	All outputs (Note 2)	-1.89	-1.675	-1.85	-	-1.65	-1.825	-1.615	V	-	Data inputs	-	-	2,12,16	7,21,22
Logic '1' threshold voltage	V_{OHA}	All outputs (Note 2)	-1.08	-	-0.98	-	-	-0.91	-	V	-	-	Data inputs	-	2,12,16	7,21,22
Logic '0' threshold voltage	V_{OLA}	All outputs (Note 2)	-	-1.655	-	-	-1.63	-	-1.595	V	-	-	-	Data inputs		
SWITCHING TIMES											**+1.11V**	**+0.3V**	**Pulse in**	**Pulse out**	**-3.2V**	**+2.0V**
Clock input propagation delay	t_{d+}	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.4	ns	Data inputs	-	Clock inputs	Outputs	2,12,16	7,21,22
	t_{d-}	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.4	ns	-	Data inputs	Clock inputs	Outputs	2,12,16	7,21,22
Rise time (20 % - 80 %)	t_r	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.3	ns	Data inputs	-	Clock inputs	Outputs	2,12,16	7,21,22
Fall time (20 % - 80 %)	t_f	All outputs	1.0	3.0	1.0	2.0	3.0	1.1	3.3	ns	-	Data inputs	Clock inputs	Outputs	2,12,16	7,21,22
Set propagation delay	t_{set}	All outputs	1.5	4.0	1.5	2.5	4.0	1.4	4.5	ns	-	-	Set inputs	Outputs	2,12,16	7,21,22
Reset propagation delay	t_{reset}	All outputs	1.5	4.0	1.5	2.5	4.0	1.4	4.5	ns	-	-	Reset inputs	Outputs	2,12,16	7,21,22
Set up time	t_s	Data inputs	1.5	-	1.5	-	-	1.5	-	ns	-	-	Data,Clock	Outputs	2,12,16	7,21,22
Hold time	t_h	Data inputs	1.0	-	1.0	-	-	1.0	-	ns	-	-	Data,Clock	Outputs	2,12,16	7,21,22
Max.clock frequency	f_{CLK}	All outputs	-	-	200	-	-	-	-	MHz	Data inputs	-	Clock inputs	Outputs	2,12,16	7,21,22

NOTES
1. Each input pin tested individually.
2. Output level to be measured after a clock pulse has been applied.

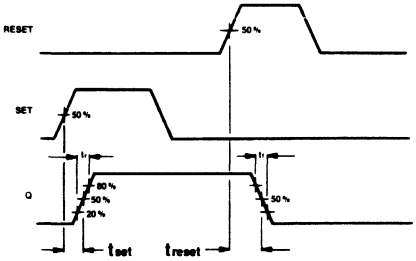




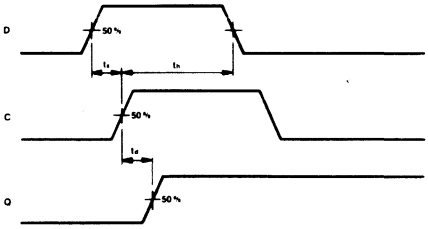
50 ohm to ground located in each scope channel input. All input and output cables to the scope are equal length of 50 ohm coaxial cable. Wire length should be ¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin.

With supply voltages at 2V and -3.2V outputs should be terminated with 50 ohms to ground; this results in an output level translation giving V_{OH} = 1.11V and V_{OL} = +0.31V.

SET AND RESET TIMING DIAGRAM



CLOCK AND DATA TIMING DIAGRAM



NOTE

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at data input (D).

Fig.3 Test circuit details for dynamic test

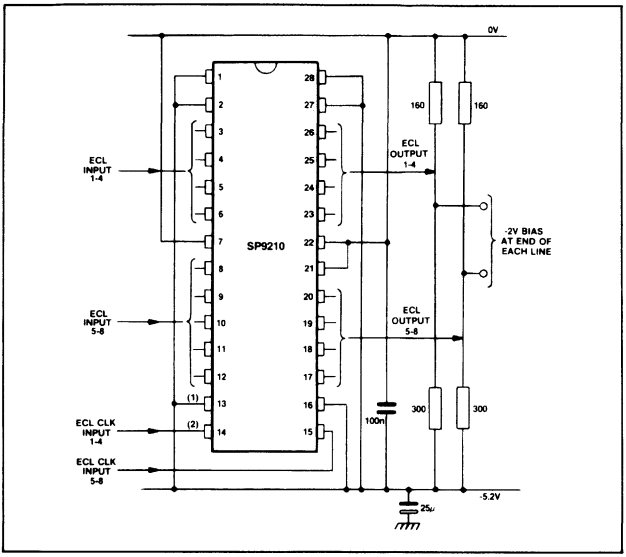


Fig.4 ECL 4 x 4 latch with 100Ω output termination

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SP9215

10-BIT 50MHz ECL UP/DOWN COUNTER

The Plessey SP9215 is an ECL compatible 10-bit Synchronous UP/DOWN Counter capable of operating at clock frequencies in excess of 50MHz. The circuit is designed to operate in preset, hold, count up, and count down modes selected by two control inputs. A count enable input and terminal count output enable counters to be cascaded with no additional components. The terminal count output goes low when the counter reaches the all 'ones' stated (count up) or the all 'zeros' state (count down). Outputs change state on the positive edge of the clock pulse.

The circuit operates from a -5.2 volt power supply and is packaged in 28-lead dual-in-line package.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

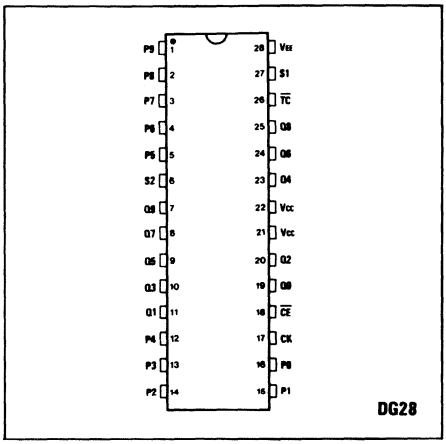


Fig.1 Pin connections - top view

FEATURES

- Fully Synchronous
- Easily Cascadable
- Presettable for Programmable Applications
- Maximum Clock Frequency in Excess of 50MHz
- Power Consumption 800mW Typical
- Functionally Similar to F10136
- Operating Temperature Range -30°C to +85°C
- -5.2V Supply

CONTROL TRUTH TABLE

$\overline{CE}$	S1	S2	Mode	$\overline{TC}$
X	L	L	Preset	H
L	L	H	Count Up	Note 1
L	H	L	Count Down	Note 1
X	H	H	Hold	H
H	L	H	Hold	H
H	H	L	Hold	H

NOTE
$\overline{TC}$ is normally High and goes Low on the terminal count.

PIN NAMES

Pn	Preset Data Inputs
Qn	Outputs
S1	Control Input
S2	Control Input
$\overline{CK}$	Clock Input
$\overline{CE}$	Count Enable
$\overline{TC}$	Terminal Count
V_{CC}	Positive Supply (Ground)
V_{EE}	Negative Supply

ELECTRICAL CHARACTERISTICS

Each circuit has been designed to meet the d.c. specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100 ohm resistor to -2 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

TEST VOLTAGE (V)					
Test temp.	V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}
-30° C	-0.890	-1.890	-1.205	-1.500	-5.2
+25° C	-0.810	-1.850	-1.105	-1.475	-5.2
+85° C	-0.700	-1.825	-1.035	-1.440	-5.2

Test Limits

Characteristic	Symbol	Pin under test	-30°C		+25°C			+85°C		Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					Vcc (GND)
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.		V_{IH} Max.	V_{IL} Min.	V_{IHA} Min.	V_{ILA} Max.	V_{EE}	
POWER SUPPLY																
Drain current	I_{EE}	28	-	-	-	-	195	-	-	mAdc	-	-	-	-	28	21,22
Input current	I_{INH}	All inputs	-	-	-	-	450	-	-	µAdc	Note 1	-	-	-	28	21,22
Input leakage current	I_{INL}	All inputs	-	-	0.5	-	-	-	-	µAdc	-	Note 1	-	-	28	21,22
Logic '1' output voltage	V_{OH}	All outputs Note 2	-1.060	-0.890	-0.960	-	-0.810	-0.89	-0.700	Vdc	Data inputs	6,27	-	-	28	21,22
Logic '0' output voltage	V_{OL}	All outputs Note 2	-1.89	-1.675	-1.85	-	-1.650	-1.825	-1.615	Vdc	-	6,27	-	-	28	21,22
Logic '1' threshold voltage	V_{OHA}	All outputs Note 2	-1.080	-	-0.98	-	-	-0.910	-	Vdc	-	6,27	Data inputs	-	28	21,22
Logic '0' threshold voltage	V_{OLA}	All outputs Note 2	-	-1.655	-	-	-1.630	-	-1.595	Vdc	-	6,27	-	Data inputs	28	21,22
SWITCHING TIMES (50 ohm load)											**+1.11V**	**+0.31V**	**Pulse in**	**Pulse out**	**-3.2V**	**+2.0V**
Propagation delay																
Clock input	t_{d} -	All outputs	-	-	2	12	20	-	-	ns	Data inputs	-	CK	Outputs	28	21,22
	t_{d}-	All outputs	-	-	2	8	15	-	-	ns	-	-	CK	Outputs	28	21,22
	t_{dT} -	$\overline{TC}$	-	-	2	10	15	-	-	ns	S2	-	CK	$\overline{TC}$	28	21,22
	t_{dT}-	$\overline{TC}$	-	-	2	10	15	-	-	ns	S2	-	CK	$\overline{TC}$	28	21,22
Count enable - terminal count	t_{dc}-	$\overline{TC}$	-	-	2	5	9	-	-	ns	S2	-	$\overline{CE}$	$\overline{TC}$	28	21,22
Set-up time																
Data inputs	t_{SHD}	All outputs	-	-	2.0	-	-	-	-	ns	-	-	CK,DATA	Outputs	28	21,22
	t_{SLD}	All outputs	-	-	2.0	-	-	-	-	ns	-	-	CK,DATA	Outputs	28	21,22
Select inputs	t_{SHS}	All outputs	-	-	5.0	-	-	-	-	ns	-	-	S1,S2,CK	Outputs	28	21,22
	t_{SLS}	All outputs	-	-	5.0	-	-	-	-	ns	-	-	S1,S2,CK	Outputs	28	21,22
Count enable input	t_{SHC}	$\overline{TC}$	-	-	5.0	-	-	-	-	ns	-	-	$\overline{CE}$,CK	$\overline{TC}$	28	21,22
	t_{SLC}	$\overline{TC}$	-	-	5.0	-	-	-	-	ns	-	-	$\overline{CE}$,CK	$\overline{TC}$	28	21,22
Hold time																
Data inputs	t_{HHD}	All outputs	-	-	-2.0	-	-	-	-	ns	-	-	CK,DATA	Outputs	28	21,22
	t_{HLD}	All outputs	-	-	-2.0	-	-	-	-	ns	-	-	CK,DATA	Outputs	28	21,22
Select inputs	t_{HHS}	All outputs	-	-	-2.0	-	-	-	-	ns	-	-	S1,S2,CK	Outputs	28	21,22
	t_{HLS}	All outputs	-	-	-2.0	-	-	-	-	ns	-	-	S1,S2,CK	Outputs	28	21,22
Count enable input	t_{HHC}	$\overline{TC}$	-	-	-2.0	-	-	-	-	ns	-	-	$\overline{CE}$,CK	$\overline{TC}$	28	21,22
	t_{HLC}	$\overline{TC}$	-	-	-2.0	-	-	-	-	ns	-	-	$\overline{CE}$,CK	$\overline{TC}$	28	21,22
Maximum counting frequency	f_{up}	$\overline{TC}$	-	-	50	-	-	-	-	MHz	S2	-	CK	All outputs	28	21,22
	f_{down}	$\overline{TC}$	-	-	50	-	-	-	-	MHz	S1	-	CK	All outputs	28	21,22
Rise time 20 % - 80 %	t_r	All outputs			1.5	3.5	5.5			ns	S2	-	CK	All outputs	28	21,22
Fall time 20 % - 80 %	t_f	All outputs			1.5	3.0	5.0			ns	S2	-	CK	All outputs	28	21,22

NOTES
1. Each input pin tested individually.
2. Output level to be measured after a clock pulse has been applied.

TEST CIRCUIT DETAILS

NOTE

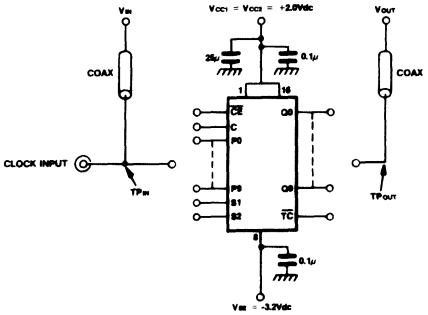
t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

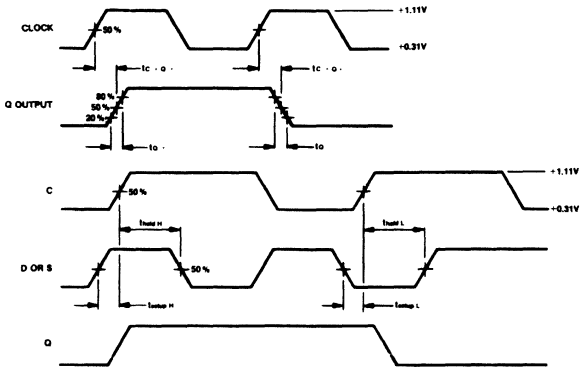
t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.

Input Pulse

t+ = t- = 2.0 ± 0.2ns

(20 to 80%)



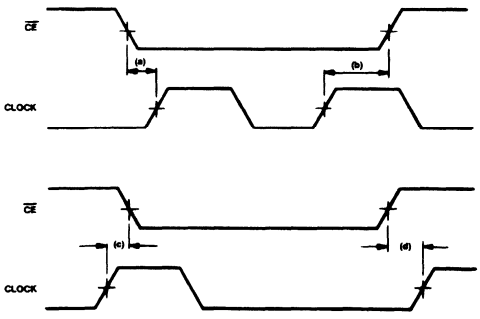


50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be <¼ inch from TP_{IN} to input pin and TP_{OUT} to output pin.

Unused outputs are connected to a 50 ohm resistor to ground.

Fig.2 Switching time test circuit and waveforms at 25° C



(a) is the minimum time to wait after the counter has been enabled to clock it

(b) is the minimum time before the counter has been disabled that it may be clocked

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter

(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter

(b) and (c) may be negative numbers

Fig.3 Set up and hold times

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SP9218

8 BIT ECL LATCHED ADDER

Voltage levels are ECL compatible. Input pull-down resistors eliminate the need to tie unused inputs to V_{EE}.

FEATURES

- 25nsec Maximum Add Time
- Input and Output Latches
- 25MHz System Operation (100MHz in Multiplex Mode)
- B Latch can be Externally Reset
- Latches can be Clocked Individually
- -30°C to +85°C Operation
- -5.2V Supply

APPLICATIONS

- Pipelined Systems
- Digital Noise Reduction
- Video Picture Enhancement
- Adder/Subtractor or Accumulator

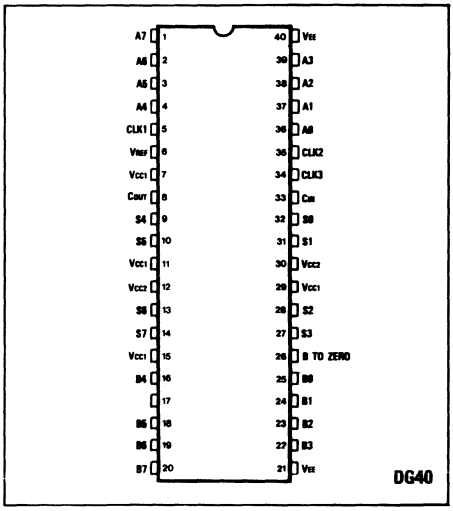


Fig.1 Pin connections - top view

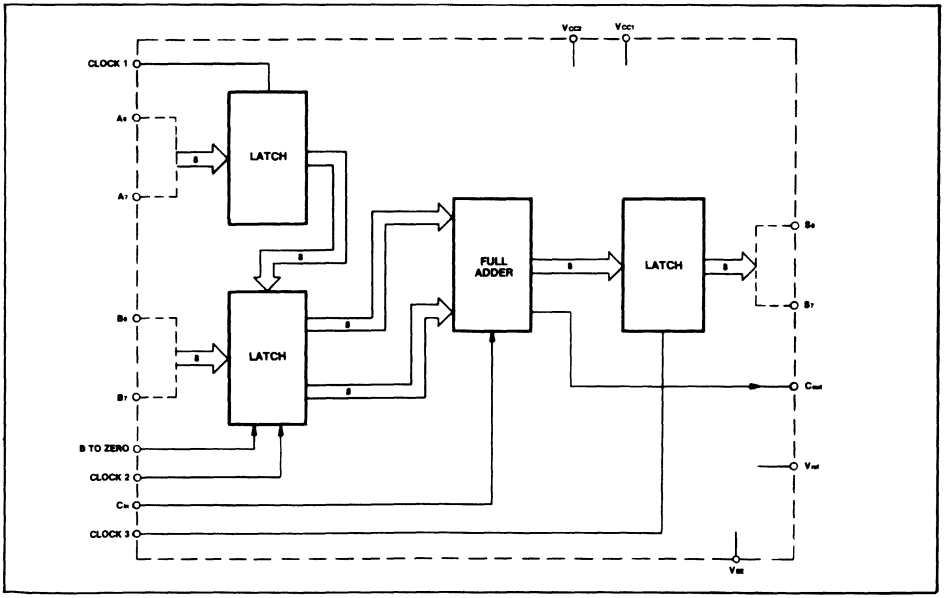


Fig.2 Internal block diagram

ELECTRICAL CHARACTERISTICS

Each circuit has been designed to meet the d.c. specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100 ohm resistor to -2 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

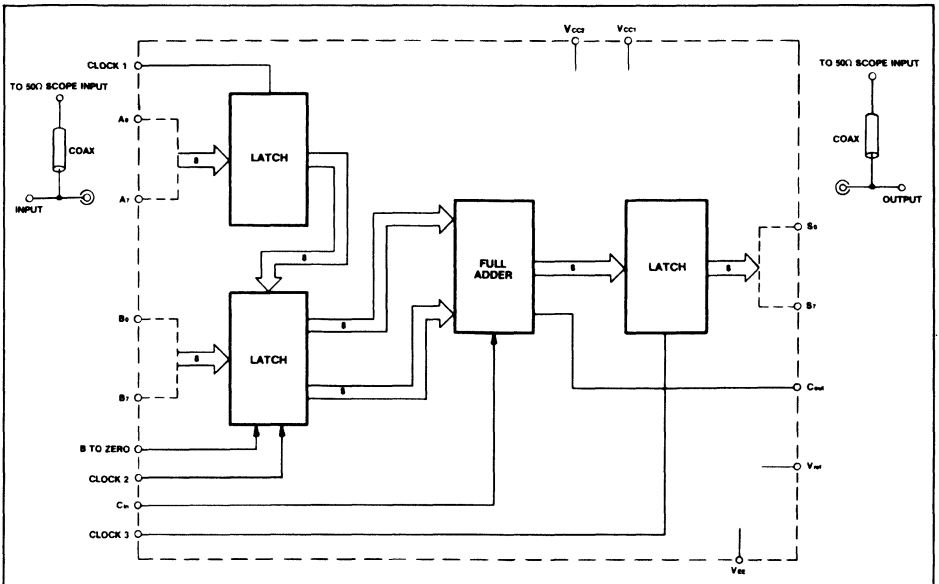
Test temp.	TEST VOLTAGES (V) V_{IH} Max.	V_{IL} Min.	V_{OHA} Min.	V_{OLA} Max.	V_{EE}
-30° C	-0.890	-1.89	-1.205	-1.500	-5.2
+25° C	-0.810	-1.85	-1.105	-1.475	-5.2
+85° C	-0.700	-1.825	-1.035	-1.440	-5.2

Characteristic	Symbol	Pin under test	-30° C Min.	-30° C Max.	+25° C Min.	+25° C Typ.	+25° C Max.	+85° C Min.	+85° C Max.	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} MAX.	V_{IL} MIN.	V_{OHA} MIN.	V_{OLA} MAX.	V_{EE}	V_{CC} -(GND)
POWER SUPPLY																
Drain current	I_{EE}	21,40	-		-	160	195	-		mA	-	-	-	-	21,40	7,11,12, 15,29,30
Input current	I_{INH}	A_{0-7};B_{0-7}	-		-		350	-		µA	Note 1	-	-	-	21,40	7,11,12, 15,29,30
		B to Zero	-		-		350	-		µA	B to Zero	-	-	-	21,40	7,11,12, 15,29,30
		CLK 1,2,3	-		-		350	-		µA	Note 1	-	-	-	21,40	7,11,12, 15,29,30
		C_{IN}	-		-		450	-		µA	C_{IN}	-	-	-	21,40	7,11,12, 15,29,30
Input leakage current	I_{INL}	C_{IN}	0.5	-	0.5	-	-	0.5	-	µA	-	Note 1	-	-	21,40	7,11,12, 15,29,30
Logic '1' output voltage	V_{OH}	All outputs	-1.06	-0.89	-0.96	-	-0.81	-0.89	-0.70	V	Note 2	Note 2	-	-	21,40	7,11,12, 15,29,30
Logic '0' output voltage	V_{OL}	All outputs	-1.89	-1.675	-1.85	-	-1.65	-1.825	-1.615	V	Note 2	Note 2	-	-	21,40	7,11,12, 15,29,30
Logic '1' threshold voltage	V_{OHA}	All outputs	-1.08	-	-0.98	-	-	-	-	V	-	-	A inputs	B inputs	21,40	7,11,12, 15,29,30
Logic '0' threshold voltage	V_{OLA}	All outputs	-	-1.655	-	-	-1.63	-	-1.595	V	-	-	B to Zero	A inputs	21,40	7,11,12, 15,29,30
ECL reference voltage	V_{ref}	6	-	-	-1.23	-1.29	-1.35	-	-	V	-	-	-	-	21,40	7,11,12, 15,29,30
SWITCHING TIMES											+1.11V	+0.31V	Pulse in	Pulse out	-3.2V	V_{CC} = +2.0V
Propagation delays																
A_0 to S_0 High	t_{a+}	S_0			5	15	20			ns	-	-	A_0	S_0	21,40	7,11,12, 15,29,30
Low	t_{a-}	S_0			5	15	20			ns	-	-	A_0	S_0	21,40	7,11,12, 15,29,30
B_0 to S_0 High	t_{a+}	S_0			5	13	18			ns	-	-	B_0	S_0	21,40	7,11,12, 15,29,30
Low	t_{a-}	S_0			5	13	18			ns	-	-	B_0	S_0	21,40	7,11,12, 15,29,30
A_0 to S_7 High	t_{a+}	S_7			5	20	25			ns	A_1-A_7	-	A_0	S_7	21,40	7,11,12, 15,29,30
Low	t_{a-}	S_7			5	20	25			ns	A1-A7	-	A_0	S7	21,40	7,11,12, 15,29,30
B_0 to S_7 High	t_{a+}	S_7			5	18	23			ns	B1-B7	-	B_0	S_7	21,40	7,11,12, 15,29,30
Low	t_{a-}	S_7			5	18	23			ns	B1-B7	-	B_0	S_7	21,40	7,11,12, 15,29,30
A_0 to C_{out} High	t_{a+}	C_{out}			5	20	25			ns	B inputs	-	A_0	C_{OUT}	21,40	7,11,12, 15,29,30
Low	t_{a-}	C_{out}			5	22	28			ns	B inputs	-	A_0	C_{OUT}	21,40	7,11,12, 15,29,30
B_0 to C_{out} High	t_{ac+}	C_{out}			5	18	23			ns	A inputs	-	B_0	C_{OUT}	21,40	7,11,12, 15,29,30
Low	t_{ac-}	C_{out}			5	20	26			ns	A inputs	-	B_0	C_{OUT}	21,40	7,11,12, 15,29,30
C_{IN} to C_{out} High	t_{acx+}	C_{out}			5	9	14			ns	A inputs	-	C_{IN}	C_{OUT}	21,40	7,11,12, 15,29,30
Low	t_{acx-}	C_{out}			5	15	20			ns	A inputs	-	C_{IN}	C_{OUT}	21,40	7,11,12, 15,29,30
Max.clock frequencies					25					MHz						
Latch enable delays																
CLK1 to S_0	t_{CK1}	S_0			5	17	22			ns	-	-	CLK1, A_0	S_0	21,40	7,11,12, 15,29,30
CLK2 to S_0	t_{CK2}	S_0			5	15	20			ns	-	-	CLK2, B_0	S_0	21,40	7,11,12, 15,29,30
CLK3 to S_0	t_{CK3}	S_0			3	9	15			ns	-	-	CLK3, A_0	S_0	21,40	7,11,12, 15,29,30
Set-up times																
A_0 to CLK1	t_{S1}	S_0			1	2.5	5.0			ns	-	-	CLK1, A_0	S_0	21,40	7,11,12, 15,29,30
B_0 to CLK2	t_{S2}	S_0			1	2.5	5.0			ns	-	-	CLK2, B_0	S_0	21,40	7,11,12, 15,29,30
A0 to CLK3	t_{S3A}	S_0			3	10	15			ns	-	-	CLK3, A_0	S_0	21,40	7,11,12, 15,29,30
B_0 to CLK3	t_{S3B}	S_0			2	8	13			ns	-	-	CLK3, B_0	S_0	21,40	7,11,12, 15,29,30
Rise time 20 %-80 %	t_r	All outputs			1	2	3.5			ns	Note 3	-	Note 3	All outputs	21,40	7,11,12, 15,29,30
Fall time 20 %-80 %	t_f	All outputs			1	2	3.5			ns	Note 3	-	Note 3	All outputs	21,40	7,11,12, 15,29,30

NOTES
1. Inputs tested one at a time.
2. Inputs applied to exercise each output.
3. Inputs and pulse applied to exercise each output.

PIN NAMES

A_{0-7}	A Data inputs
B_{0-7}	B Data inputs
S_{0-7}	Summed outputs
C_{in}	Carry input
C_{out}	Carry output
CLK1	Enables A data latches (low to enable)
CLK2	Enables adder input latches (low to enable)
CLK3	Enables output latches (low to enable)
B to Zero	Resets outputs B adder input latches to zero
V_{CC1},V_{CC2}	Positive power supply (Ground)
V_{EE}	Negative power supply
V_{ref}	ECL reference voltage (-1.29V)



Supply voltages at 2V and -3.2V enable outputs to be terminated by 50 ohm to ground. All input and output cables to the scope are equal lengths of 50 ohm coaxial cable terminated by 50 ohm located in each scope channel input. The B to Zero is normally low, high will clear B latch.

Fig.3 Test circuit details

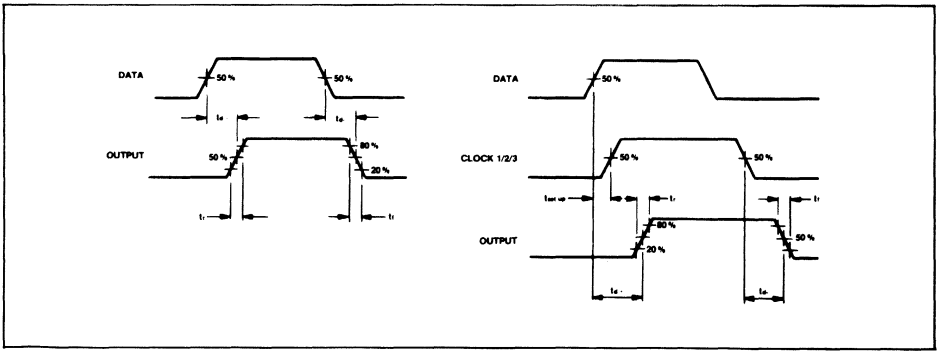


Fig.4 Timing waveforms

PLESSEY
Semiconductors

SP9680

ULTRA FAST COMPARATOR

The SP9680 is an ultra fast comparator manufactured using a high performance bipolar process which makes possible very short propagation delays (2.4ns typ.).

The circuit has differential inputs and complementary ECL outputs, capable of driving 50 Ω lines.

The device is manufactured in a low cost mini-dip package and is intended as an alternative to the faster SP9685 in applications where performance premium and the latch facility are not required.

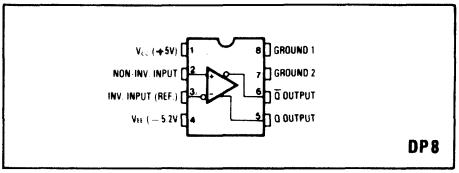


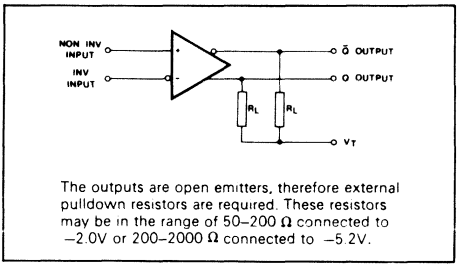
Fig. 1 Pin connections

FEATURES

- Propagation Delay 2.4ns Typ.
- Complementary ECL Outputs
- 50 Ω Line Driving Capability
- Excellent Common Mode Rejection
- 8-Lead Plastic Package

QUICK REFERENCE DATA

- Supply Voltages +5, −5.2V
- Operating Temperature Range −30°C to +70°C



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200 Ω connected to −2.0V or 200–2000 Ω connected to −5.2V.

Fig. 2 Functional diagram

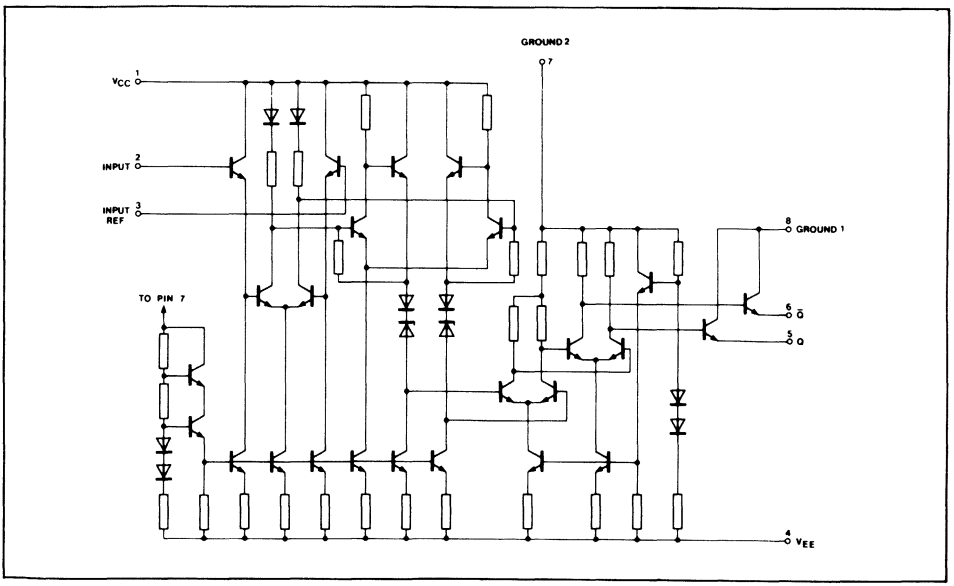


Fig. 3 SP9680 circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25°C
V_{CC} = 5.00V ± 0.25V
V_{EE} = −5.2V ± 0.25V
R_L = 50Ω
V_T = −2.0V (See Fig. 2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	−6		+6	mV	R_S <100Ω
Input bias current		20	40	μA	
Input offset current			10	μA	
Supply current I_{CC}		18	25	mA	
I_{EE}		22	35	mA	
Total power dissipation		200	300	mW	
Input to Q output delay		2.4	4	ns	} 100mV pulse,10mV overdrive
Input to $\overline{Q}$ output delay		2.4	4	ns	
Common mode range	−2		+2	V	
Common mode rejection ratio		80		dB	
Output logic levels					
Output HIGH	−0.96		−0.81	V	
Output LOW	−1.85		−1.65	V	
Input capacitance		3.5		pF	
Input resistance	50			kΩ	
Operating temperature range	−30		+70	°C	

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage V_{CC} +6V
Negative supply voltage V_{EE} −6V
Output current 30mA
Input voltage ±3V
Differential input voltage 3.5V
Storage temperature −55°C to +125°C

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SP9685

ULTRA FAST COMPARATOR

The SP9685 is an ultra-fast comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50 Ω terminated transmission lines. The high resolution available makes the device ideally suited to analogue-to-digital signal processing applications.

A latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the outputs are forced to an unambiguous ECL logic state dependent on the input conditions at the time of the latch input transition. If the latch function is not used, the latch enable may be connected to ground.

The device is pin compatible with the AM685 but operates from conventional +5V and −5.2V rails.

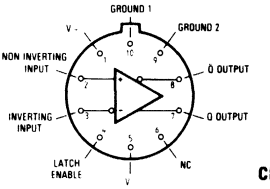
FEATURES

- Propagation Delay 2.2ns Typ.
- Latch Set-up Time 1ns Max.
- Complementary ECL Outputs
- Supply +5V, -5.2V
- Operating Temperature Range -30°C to +85°C
- 50 Ω Line Driving Capability
- Excellent Common Mode Rejection
- Pin Compatible with AM685 — But Faster

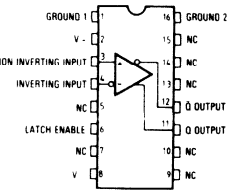
ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	6V
Negative supply voltage	−6V
Output current	30mA
Input voltage	±3V
Differential input voltage	3.5V
Power dissipation	300mW
Storage	−55°C to +150°C
Lead temperature (soldering 60 sec)	300°C

TOP VIEW



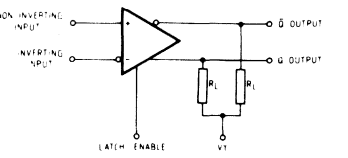
CM10/S



DG16

On CM package, pin 5 is connected to case.

Fig. 1 Pin connections



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200Ω connected to −2.0V or 200–2000Ω connected to −5.2V

Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{AMB} = 25°C
V_{CC} = +5.0V ±.25V
V_{EE} = −5.2V ±.25V
R_L = 50Ω: V_T = -2.0V (See Fig.2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	−5		+5	mV	Rs <100 Ω
Input bias current		10	20	μA	
Input offset current			5	μA	
Supply currents Icc		19	23	mA	
I_{EE}		23	34	mA	
Total power dissipation		210	300	mW	
Min. latch set-up time (t_s)		0.5	1	ns	
Input to Q output delay (t_{pd})		2.2	3	ns	100 mV pulse 10 mV overdrive
Input to $\overline{Q}$ output delay (t_{pd})		2.2	3	ns	
Latch to Q delay $t_{pd}(E)$		2.5	3	ns	
Latch to $\overline{Q}$ delay $t_{pd}(E)$		2.5	3	ns	
Min. latch pulse width $t_{pw}(E)$		2	3	ns	
Min. hold time (t_h)			1	ns	
Common mode range	−2.5		+2.5	V	
Input capacitance		3		pF	
Input resistance	60			kΩ	
Output logic levels					
Output High	−.96		−.81	V	At nominal supply voltages, see Fig. 4
Output Low	−1.85		−1.65	V	
Common mode rejection ratio	80			dB	
Supply voltage rejection ratio	60			dB	

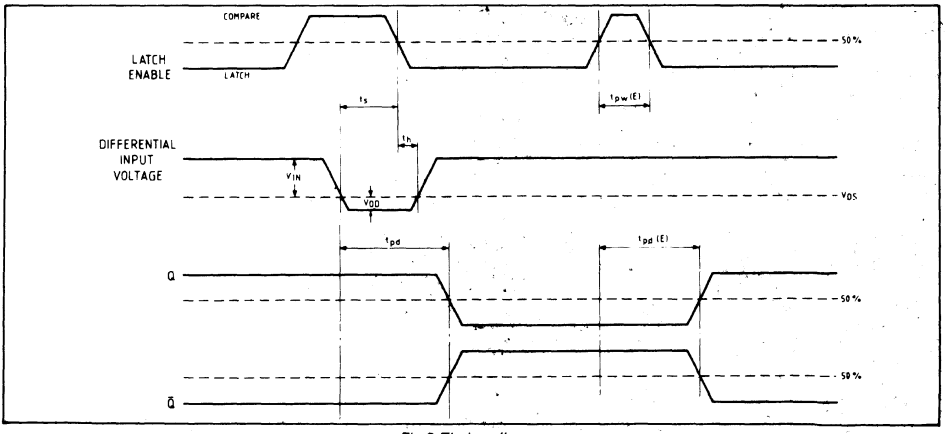


Fig.3 Timing diagram

OPERATING NOTES

Timing diagram

The timing diagram, Figure 3, shows in graphic form a sequence of events in the SP9685. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse switches the comparator over after a time tpd. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must be maintained for a time t_h after the latch falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse width $t_{pw(E)}$ is required for the strobe operation, and the output transitions occur after a time $t_{pd(E)}$.

Measurement of propagation and latch delays

A simple test circuit is shown in Figure 4. The operating sequence is:

1. Power up and apply input and latch signals. Input = 100mV square wave, latch ECL levels. Connect monitoring scope(s).
2. Select 'offset null'.

3. Adjust offset null potentiometer for an output which switches evenly between states on clock pulses.
4. Measure input/output and latch/output delays at 5mV offset, 10mV offset and 25mV offset.

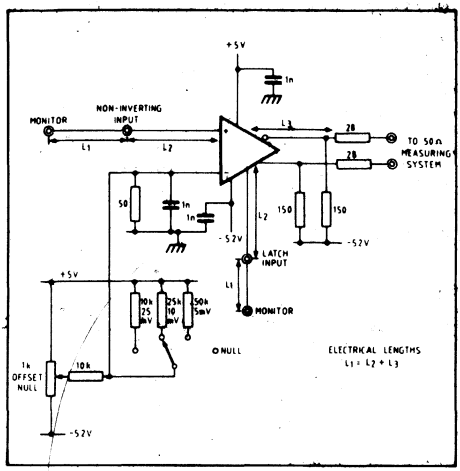


Fig.4 SP9685 test circuit

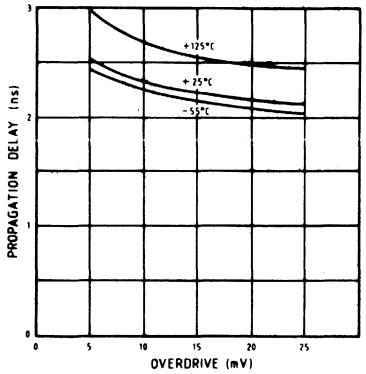


Fig.6 Propagation delay, latch to output as a function of overdrive

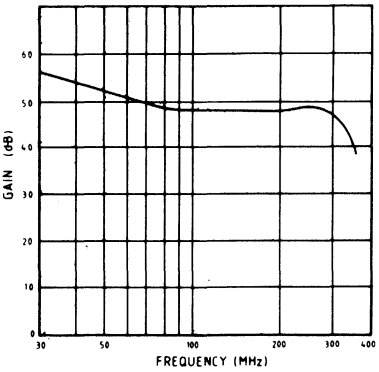


Fig.5 Open loop gain as a function of frequency

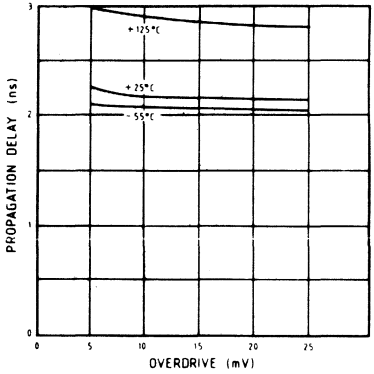


Fig.7 Propagation delay, input to output as a function overdrive

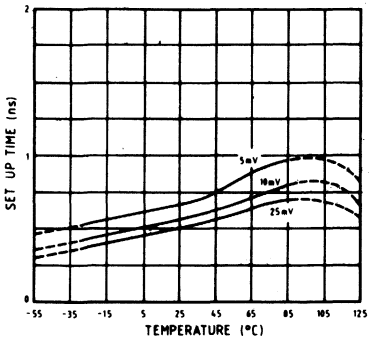


Fig.8 Set-up time as a function of temperature

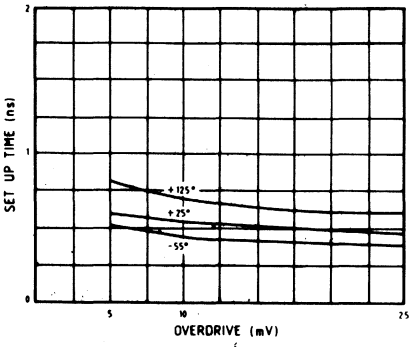


Fig.9 Set-up time as a function of input overdrive

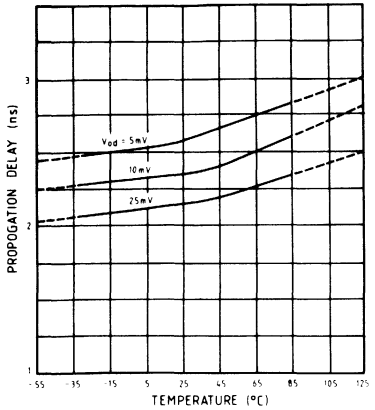


Fig.10 Propagation delay, input to output as a function of temperature

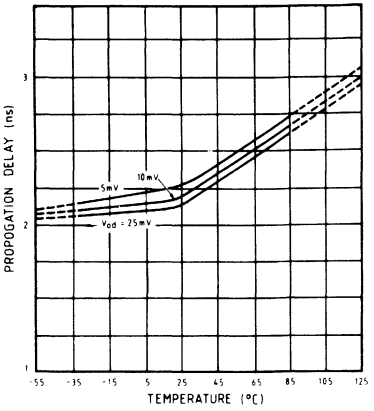


Fig.11 Propagation delay, latch to output as a function of temperature

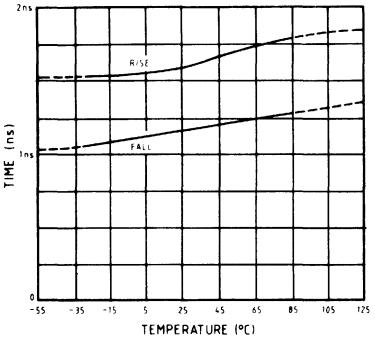


Fig.12 Output rise and fall times as a function of temperature

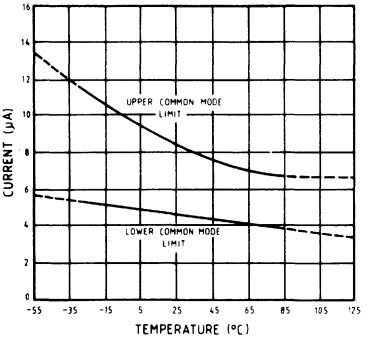


Fig.13 Input bias currents as a function of temperature

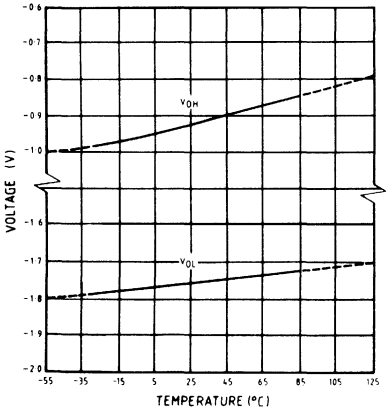


Fig.14 Output levels as a function of temperature

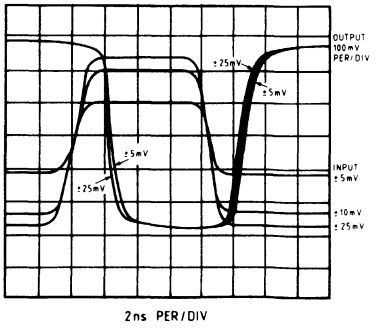


Fig.15 Response to various input signal levels

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SP9687

ULTRA FAST DUAL COMPARATOR

The SP9687 is an ultra-fast, dual comparator manufactured with a high performance bipolar process which makes possible very short propagation delays (2.2ns typ.). The circuit has differential inputs and complementary outputs fully compatible with ECL logic levels. The output current capability is adequate for driving 50Ω terminated transmission lines. The high resolution available makes the device ideally suited to analogue-to-digital signal processing applications.

A latch function is provided to allow the comparator to operate in the follow-hold or sample-hold mode. The latch function inputs are intended to be driven from the complementary outputs of a standard ECL gate. If LE is high, and $\overline{LE}$ is low, the comparator function is in operation. When LE is driven low and $\overline{LE}$ high, the outputs are locked into the logical states at the time of arrival of the latch signal. If the latch function is not used, LE must be connected to ground.

The device is pin compatible with the AM687 and operates from conventional +5V and −5.2V rails.

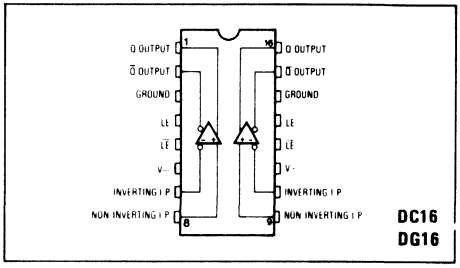


Fig. 1 Pin connections

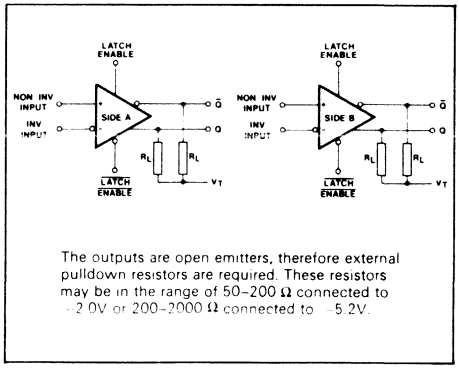


Fig. 2 Functional diagram

FEATURES

- Propagation Delay 2.2ns Typ.
- Latch Set-up Time 1ns Max.
- Complementary ECL Outputs
- 50Ω Line Driving Capability
- Excellent Common Mode Rejection
- Supply Voltages +5V, -5.2V
- Operating Temperature Range -30°C to +85°C
- Pin Compatible with AM687 — But Faster

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	6V
Negative supply voltage	6V
Output current	30mA
Input voltage	± 3V
Differential input voltage	± 3.5V
Power dissipation	590mW
Storage	−55°C to +125°C
Lead temperature (soldering 60 sec)	300°C

OPERATING NOTES

Timing diagram

The timing diagram, Figure 3, shows in graphic form a sequence of events in the SP9687. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse, switches the comparator over after a time tpd. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must be maintained for a time t_h after the latch falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse with $t_{pw(E)}$ is required for the strobe operation, and the output transitions occur after a time $t_{pd\,(E)}$. The $\overline{LE}$ input is omitted for clarity.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{AMB} = 25°C$
$V_{CC} = +5.00V \pm .25V$
$V_{EE} = -5.20V \pm .25V$
$R_L = 50\Omega$
$V_T = -2.0V$

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	−5		+5	mV	Rs <100 Ω
Input bias current		5	20	µA	
Input offset current		1	5	µA	
Supply currents Icc		30	46	mA	Note 3
IEE		54	68	mA	Nominal conditions
Total power dissipation		430	590	mW	
Min. latch set-up time (t_s)		0.5	1	ns	Notes 1,2
Input to Q output delay (t_{pd})		2.2	3	ns	100 mV pulse, note 1
Input to $\overline{Q}$ output delay (t_{pd})		2.2	3	ns	10 mV overdrive, note 1
Latch to Q delay $t_{pd}(E)$		2.5	3	ns	Notes 1,2
Latch to $\overline{Q}$ delay $t_{pd}(E)$		2.5	3	ns	
Min. latch pulse width $t_{pw}(E)$		2	3	ns	
Min. hold time (t_h)			1	ns	
Common mode range	−2.5		+2.5	V	
Input capacitance		3		pF	
Input resistance	60			kΩ	
Output logic levels					
Output High	− .96		− .81	V	At nominal supply
Output Low	−1.85		−1.65	V	voltages
Operating temperature range	−30°		+85°	°C	
Common mode rejection ratio	80			dB	
Supply voltage rejection ratio	60			dB	

NOTES
1. These measurements are defined under conditions of a +100mV pulse with −10mV overdrive. The relationship between overdrive and delay is illustrated in Figs. 6 to 8.
2. Switching measurements involving the latch are particularly difficult to perform and cannot be tested in production. Circuit analysis shows that at least 95% of devices will meet these specifications.
3. Refers to the entire package. Other data in this table applies to each half device.

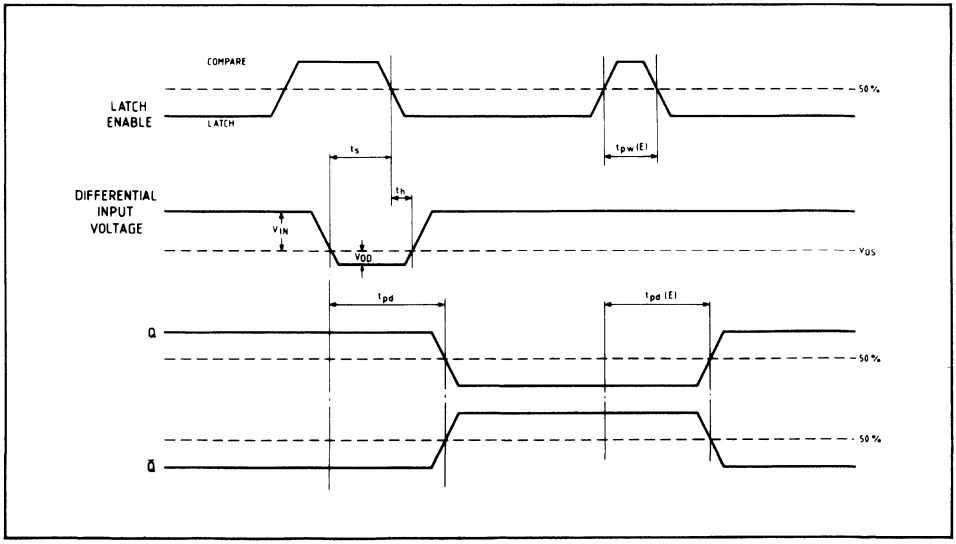


Fig. 3 Timing diagram

PERFORMANCE CURVES

Unless otherwise specified, standard conditions for all curves are $T_{AMB} = 25°C$, $V_{CC} = 5.0V$, $V_{EE} = -5.2V$

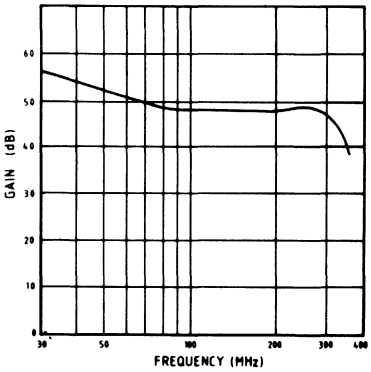


Fig. 4 Open loop gain as a function of frequency

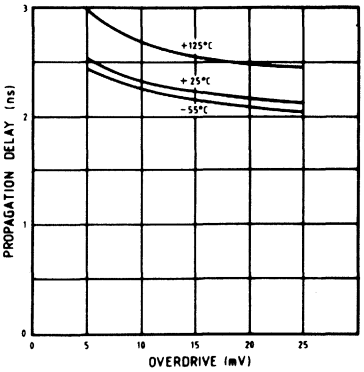


Fig. 5 Propagation delay, latch to output as a function of overdrive

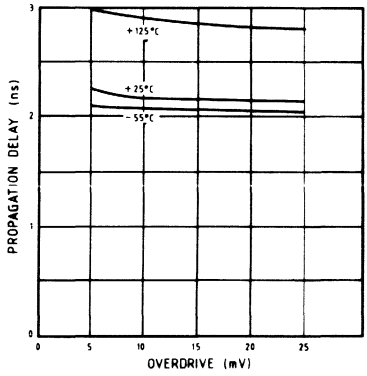


Fig. 6 Propagation delay, input to output as a function of overdrive

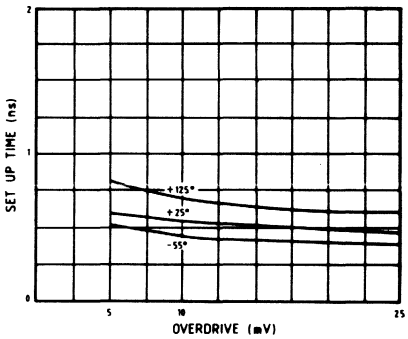


Fig. 7 Set-up time as a function of input overdrive

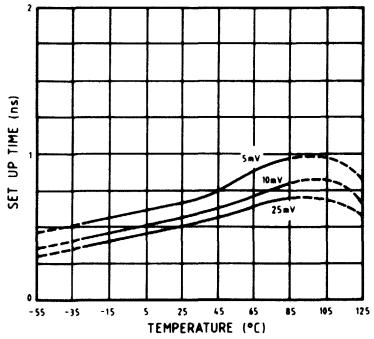


Fig. 8 Set-up time as a function of temperature

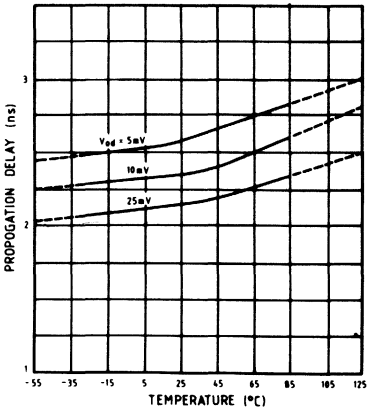


Fig. 9 Propagation delay, input to output as a function of temperature

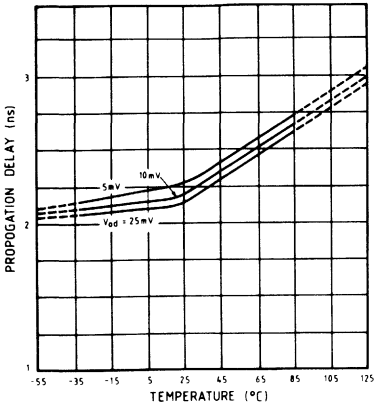


Fig. 10 Propagation delay, latch to output as a function of temperature

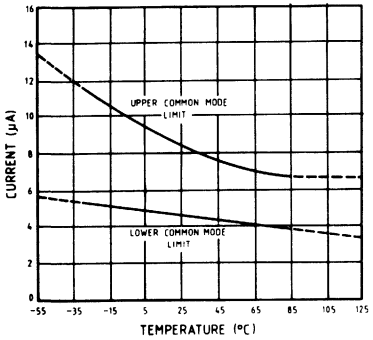


Fig. 12 Input bias currents as a function of temperature

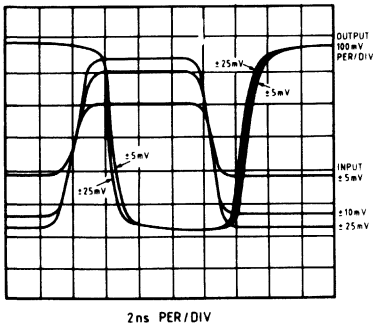


Fig. 14 Response to various input signal levels.

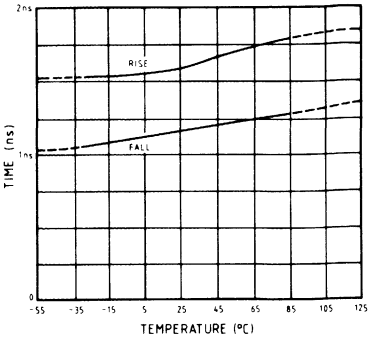


Fig. 11 Output rise and fall times as a function of temperature

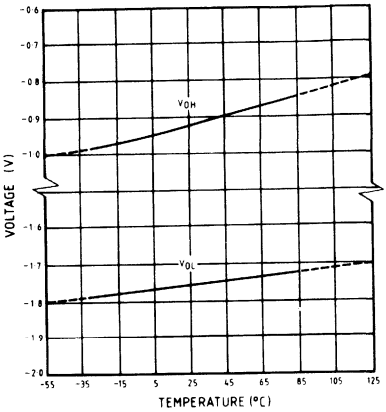


Fig. 13 Output levels as a function of temperature

PLESSEY
Semiconductors

SP9754

FOUR BIT EXPANDABLE A TO D CONVERTER

The SP9754 is a fast 4 bit A-D converter, expandable up to 8 bits without additional encoding circuitry.

It can convert at sample rates from DC to 110MHz, with analogue inputs up to Nyquist frequencies. All output levels are ECL compatible.

The latch function to the device provides on-chip sampling which allows the converter to operate without an external sample and hold. Data is clocked through the device in master/slave fashion, ensuring that all outputs are synchronous and valid for the complete clock period.

The SP9754 operates from a +5V, -7V supply.

FEATURES

- No External Components For 4-Bit Conversion
- 110MHz Conversion Rate
- On-Chip Encoding For Expansion to 8 Bits
- No External Sample and Hold Needed
- On-Chip Resistor Reference Divider
- Bit Size 10-100mV
- ECL Compatible
- Over 50MHz Full Power Bandwidth
- 10ps Aperture Uncertainty Time
- 8-Bit Accuracy

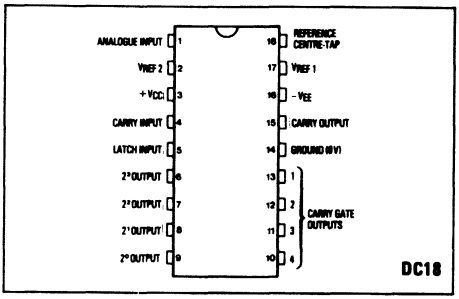


Fig.1 Pin connections

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	-7.5V
Operating temperature range	-30°C to +85°C
Storage temperature	-55°C to +125°C
Lead temperature (soldering 60s)	300°C

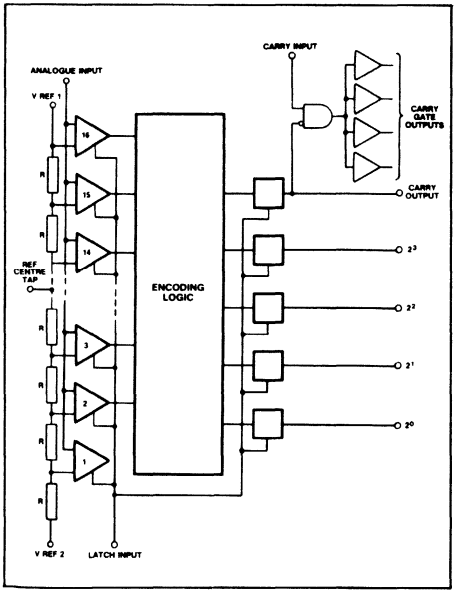


Fig.2 Functional diagram

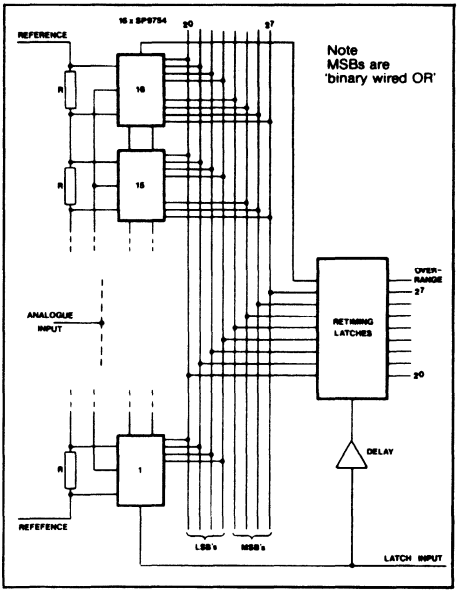


Fig.3 8-bit all-parallel system

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{AMB} = 25°C
V_{CC} = +5V ±0.25V
V_{EE} = -7V ±0.25V
R_L = 100ohms to -2V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Analogue input current	I_B		30	100	μA	V_{IN} = 0V
Analogue input capacitance	C_{IN}		10		pF	
Common mode range	V_{CM}	-2		+2	V	
Maximum input slew rate			1000		V/μsec	
Latch input capacitance	C_{IN}		2		pF	
Positive supply current	I_{CC}		55	70	mA	See Fig.11
Negative supply current	I_{EE}		85	100	mA	
Reference resistor chain			25		Ω	
Reference bit size		10		100	mV	
Comparator offset voltage	V_{OS}	-5		+5	mV	
Total power dissipation	P_{DISS}		950	1160	mW	All outputs loaded
Output logic levels						
Logic high	V_{OH}	-0.930		-0.720	V	for 100 ohm load
Logic low	V_{OL}	-1.90		-1.620	V	to -2V
Min. latch set-up time	ts		1.5	2	nsec	10mV overdrive
Latch to output propagation delay:						
Latch enable to output high	t_{pd} + (E)		6	8	nsec	
Latch enable to output low	t_{pd} - (E)		5	8	nsec	
Carry input to MSB delay	t_{pd} (C)		3	5	nsec	
Max. sample rate	$F_{c\,max.}$	100	110		MHz	
Aperture uncertainty time	ta		10		psec	

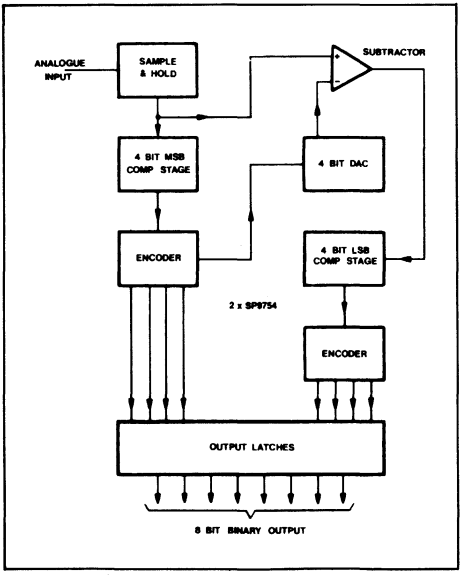


Fig.4 Parallel-series-parallel system

PERFORMANCE CURVES

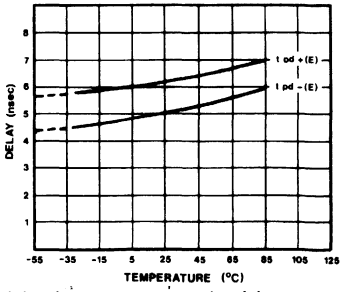


Fig.5 Latch to output propagation delay as a function of temperature

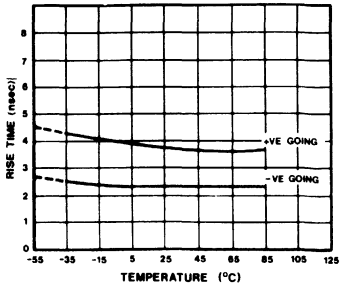


Fig.6 Output rise/fall times as a function of temperature

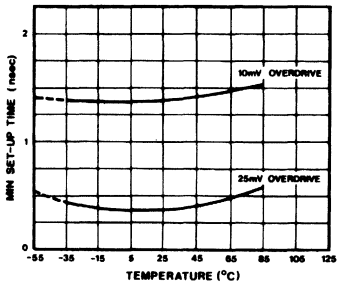


Fig.7 Set-up time as a function of temperature

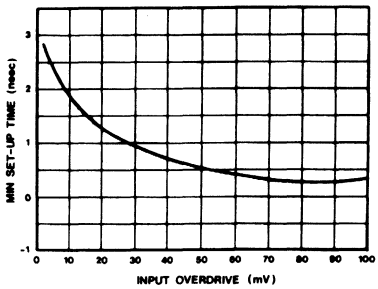


Fig.8 Set-up time as a function of overdrive

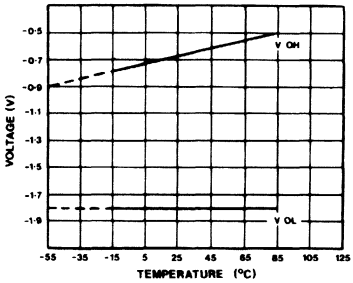


Fig.9 Output logic levels as a function of temperature

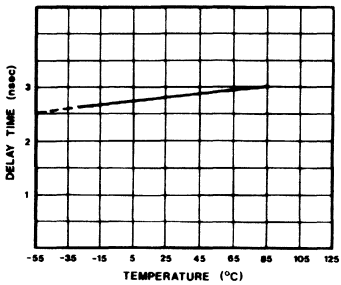


Fig.10 Carry input to MSB output delay as a function of temperature

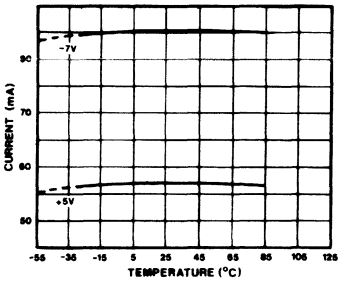


Fig.11 Supply current as a function of temperature

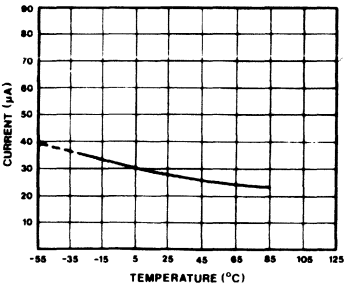


Fig.12 Analogue input current as a function of temperature

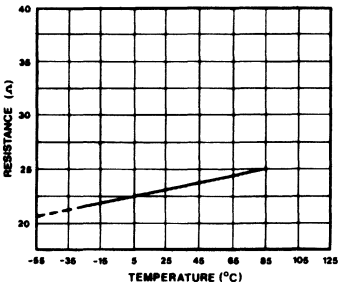


Fig.13 Network resistance as a function of temperature

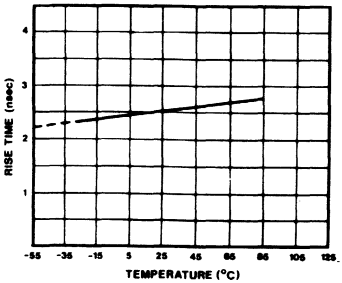


Fig.14 MSB output edge speeds as a function of temperature

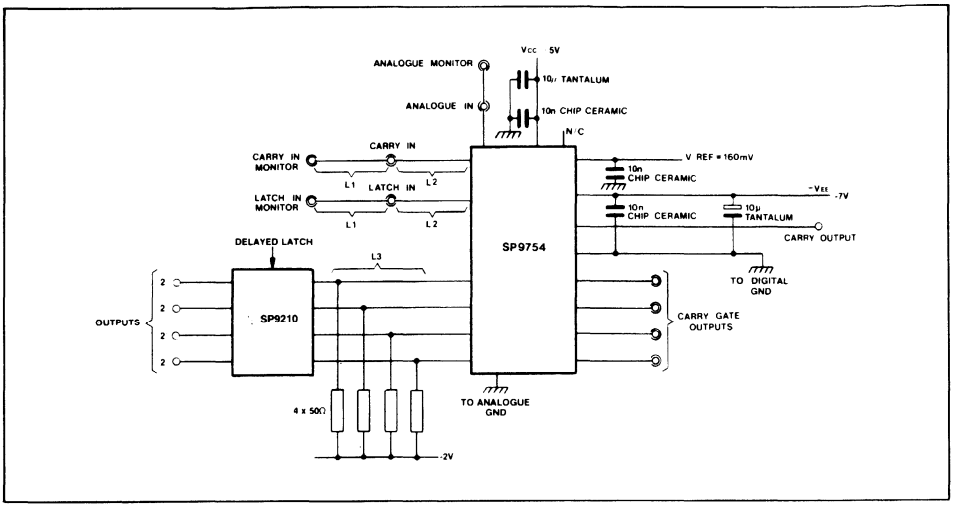


Fig.15 High frequency test circuit
NOTE At latch frequencies below 60MHz the SP9210 can be ommitted.

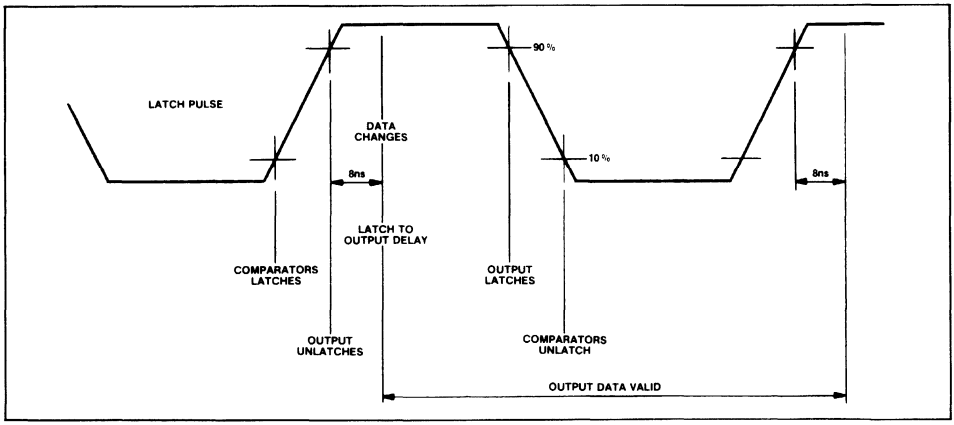


Fig.16 Timing diagram

OPERATING NOTES

1. Carry output (pin 15) is high when the analogue input exceeds the top reference voltage (pin 17).

Then the carry gate outputs (pins 10 to 13) go low regardless of carry input (pin 4). When the analogue input is between V_{REF} and V_{REF2} and the carry output is low, the carry gate output will be high if the carry input is also high. Similarly if the carry input is low then the carry gate outputs will be low.

2. When used in an ambient temperature in excess of 45° C the SP9754 must be provided with an external electrically isolated heatsink or forced air cooling. This will ensure that the junction temperature does not exceed 150° C (thermal resistance junction/case 35° C per watt).

PLESSEY
Semiconductors

SP9768

8 BIT DIGITAL TO ANALOGUE CONVERTER

The SP9768 is capable of converting an 8-bit digital signal into an analogue voltage at a rate of over 100 mega-samples per second. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. Included on the chip are a precision voltage reference and a reference amplifier.

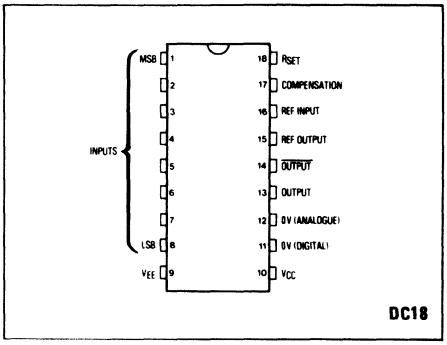


Fig.1 Pin connections

FEATURES

- 5ns Setting Time to ½ LSB
- ECL Inputs, Current Output
- Voltage Reference Temp. Coeff. 50 ppm/°C
- Over 100 MBits/S Update Rate
- 40MHz Multiplying Mode
- Operating Temperature Range -30°C to +85°C

APPLICATIONS

- Data Conversion
- Instrumentation
- Video Speed Successive Approximation ADCs
- Video Graphic Displays

QUICK REFERENCE DATA

Supply voltages: +5V, -5.2V
Power consumption: 400mW

ABSOLUTE MAXIMUM RATINGS

Supply voltage: -6V, +6V
Storage temperature: -55°C to +125°C
Operating temperature range: -30°C to +85°C

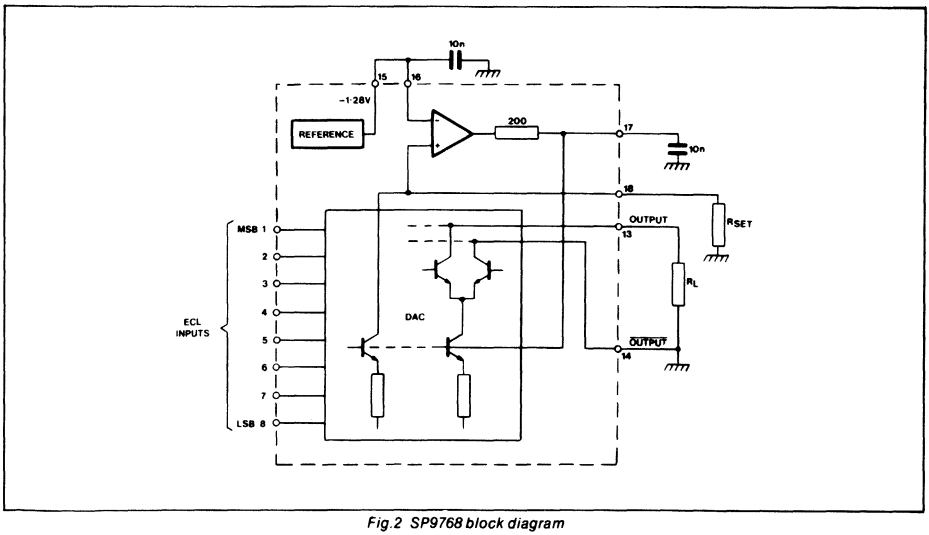


Fig.2 SP9768 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 25°C
V_{CC} +5.00V ±5%
V_{EE} -5.20V ±5%
R_L = 50Ω
R_{set} = 220Ω
Input voltage High -0.96V (min) -0.81V (max)
Low -1.85V (min) -1.65V (max)

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Differential non-linearity			0.2	%	
Absolute non-linearity			0.2	%	
Settling time		5		ns	See Operating Note 1
Nominal bit size		78		μA	R_L = 50Ω } R_{set} = 220Ω
		4		mV	
Positive output compliance		+3		V	
Negative output compliance	-1			V	25°C see Operating Note 2
	-0.7			V	+85°C
Multiplying bandwidth		40		MHz	Current mode, see Operating Note 3
Maximum full scale output		30		mA	
Minimum full scale output		2		mA	
Reference voltage		-1.28		V	
Temp coeff of reference voltage		20		ppm/°C	
Zero output		60		μA	
Output current symmetry		100		μA	
Supply current (I_{CC})		12	20	mA	
(I_{EE})		66	80	mA	

CIRCUIT DESCRIPTION

The DAC has current outputs, with a nominal full scale of 20mA, corresponding to a 1volt drop across a 50ohm load, or ±1volt across 100ohms returned to +1 volt. See Operating Note 2.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, I_{OUT}, is given by

$$I_{OUT} = 4 \times \frac{V_{REF}}{R_{SET}} \quad \text{at full scale}$$

A complementary $\overline{I_{OUT}}$ is also provided. The setting resistor, R_{SET}, is typically 220ohms, and should have a temperature coefficient similar to that of the output load resistor.

Where the load is an oscilloscope, with a 50ohm nominal input, a good quality metal oxide resistor should be used for R_{SET}. It is important to realise that reflections present in 50ohm load systems will often prove to be a limiting factor in the measurement of settling time.

The reference voltage source is nominally 1.280volts and is of a modified bandgap type, average temperature coefficient of 20ppm/°C over the range -55°C to +125°C, corresponding to approximately 1LSB change over this temperature range.

To reduce the possibility of instability or noise generation, the reference supply (pin 15) can be decoupled using a high quality ceramic chip capacitor. Stabilisation of the loop amplifier is by a single capacitor from pin 17 to ground. Minimum value is 3900pF, although a 10nF chip ceramic is recommended.

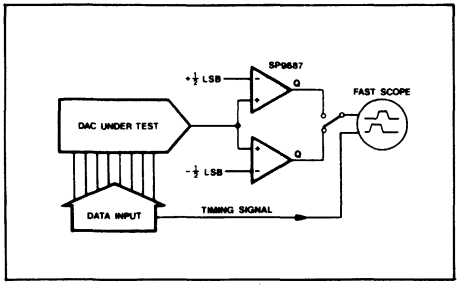


Fig.3 Test schematic (settling time)

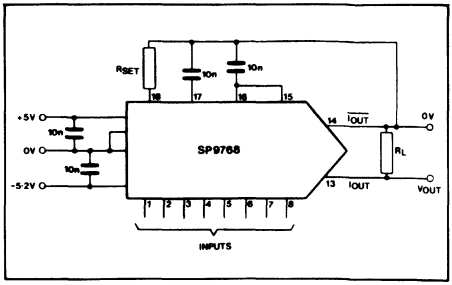


Fig.4 Conventional DAC. Negative output wrt ground.

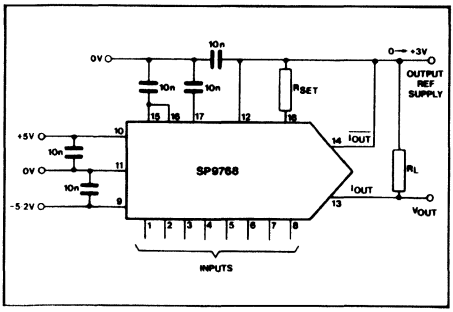


Fig.5 Voltage output referred to positive supply

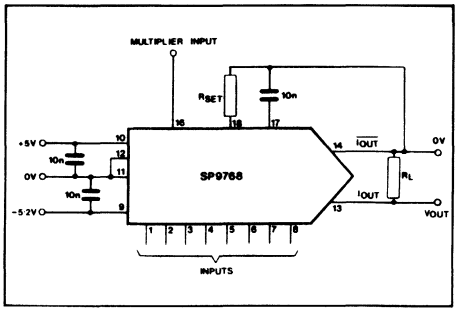


Fig.6 Multiplying DAC (Voltage mode)

OPERATING NOTES

1. Measurement of Settling Time

The settling time of the SP9768 is measured for a worst case transition of 0 to full scale.

Oscilloscopes, whether real time or sampling, do not have sufficiently low input VSWR or on-screen resolution for precise settling time measurements. A measurement technique has been designed, shown diagrammatically in Fig.3, in which the DAC can settle into a nearly ideal 50ohm load, with minimal interconnection paths; this is also very closely related to the practical use of the device. Precision settling time measurements can be performed with a high speed comparator, conveniently a dual device, such as the SP9687, with a minimal delay time, in this case about 2ns. Two references are set up to detect the DAC output settling within a window, conveniently defined as the settling to ground of the output.

The lower comparator detects the DAC output coming within ½LSB of the final settling point, while the upper device checks that there is less than ½LSB of over shoot.

2. Output Compliance

Fig.5 shows the method of using the SP9768 with a load resistor not referred to ground. This connection will be used most often when a larger output voltage than that permitted by the -0.7volt negative output voltage compliance specification is required. The output resistor can be referred to a positive supply in this case as long as R_{set} and the analogue ground are also referred to this voltage. If I_{OUT} is also connected to this reference the decoupling will be simplified.

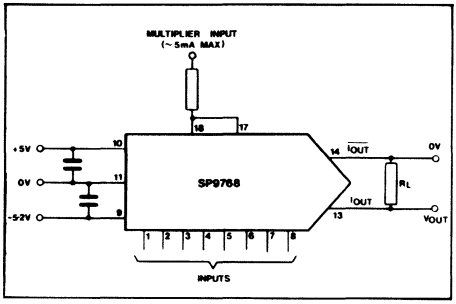


Fig.7 Multiplying DAC (Current mode)

3. Multiplication Modes

Multiplying operation of the DAC is available in two modes, either a voltage applied in place of the reference, or a current supplied via the current source pin. In the former case the 3dB bandwidth is 250kHz, while in the latter, operational use exceeds 40MHz. Suggested circuits are shown in Figs. 6 and 7.

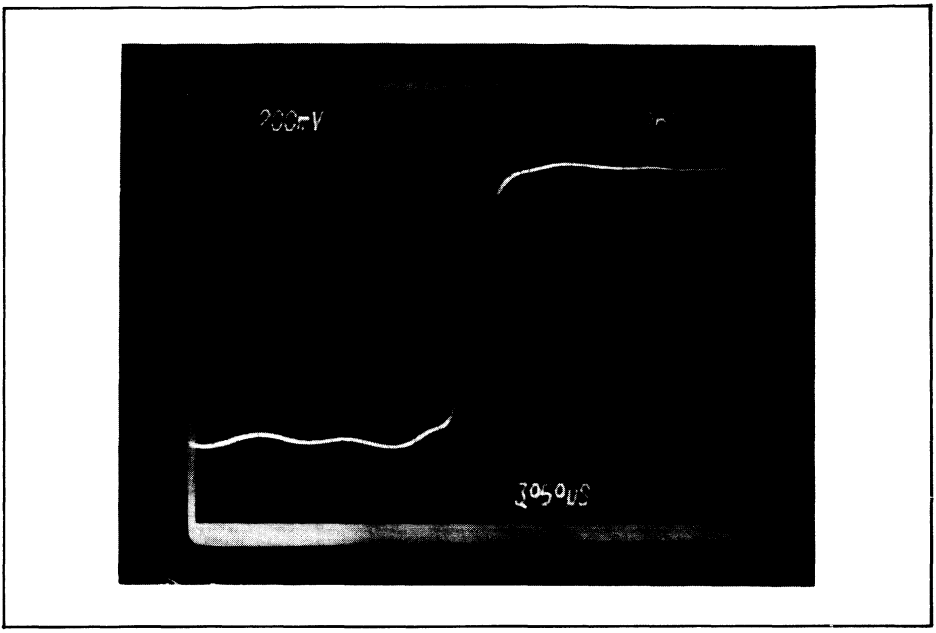


Fig. Full scale transition of I_{OUT} into 50 ohm using 1GHz bandwidth oscilloscope

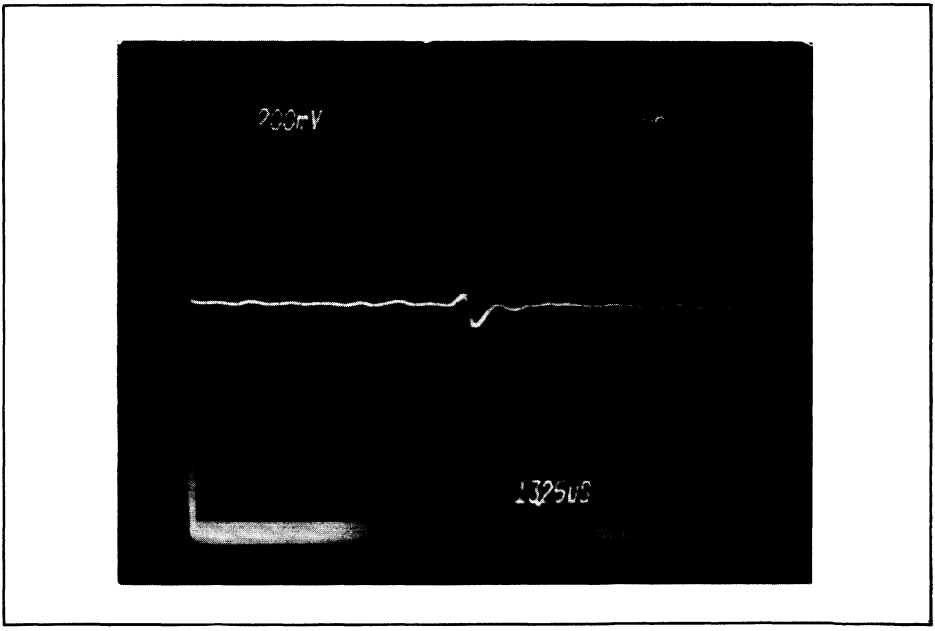
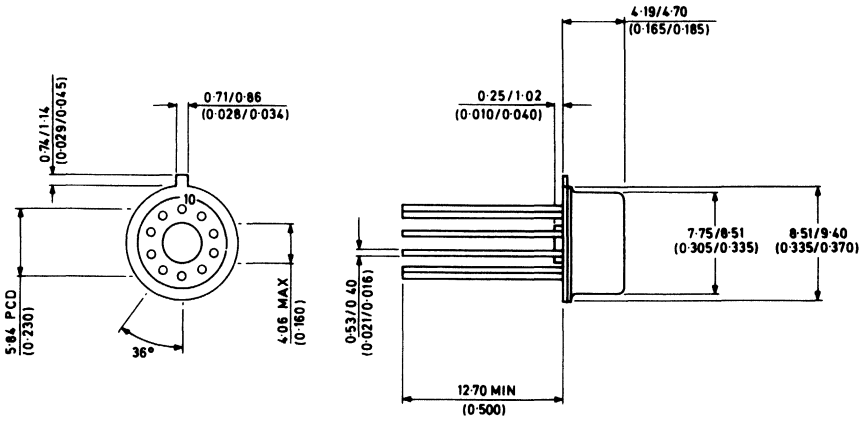
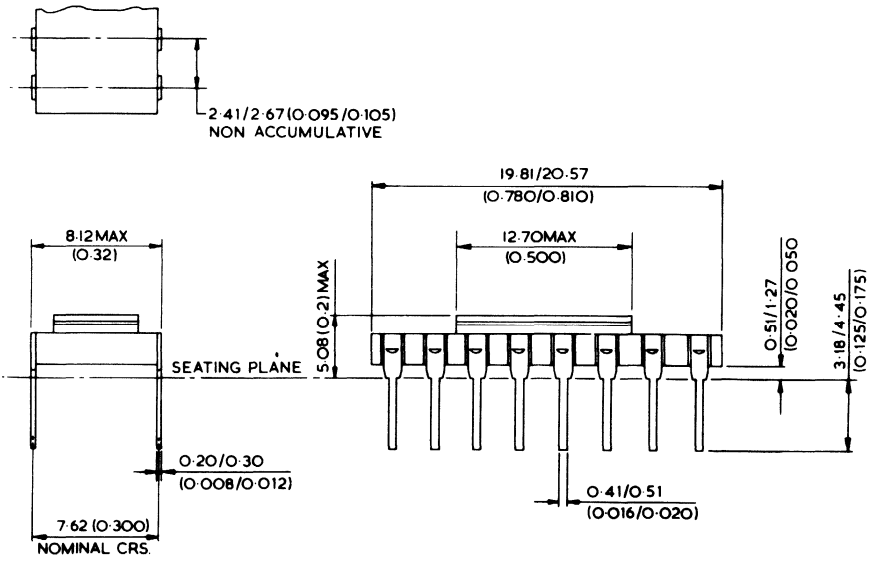


Fig. Typical centre point low energy glitch using 1GHz bandwidth oscilloscope

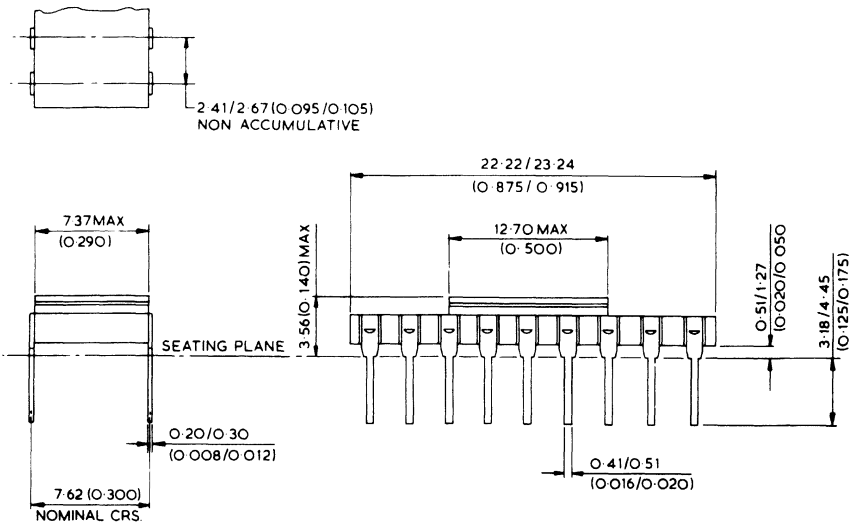
Package Outlines



10 LEAD TO-100 (5.84 mm PCD) WITH STANDOFF CM10/S

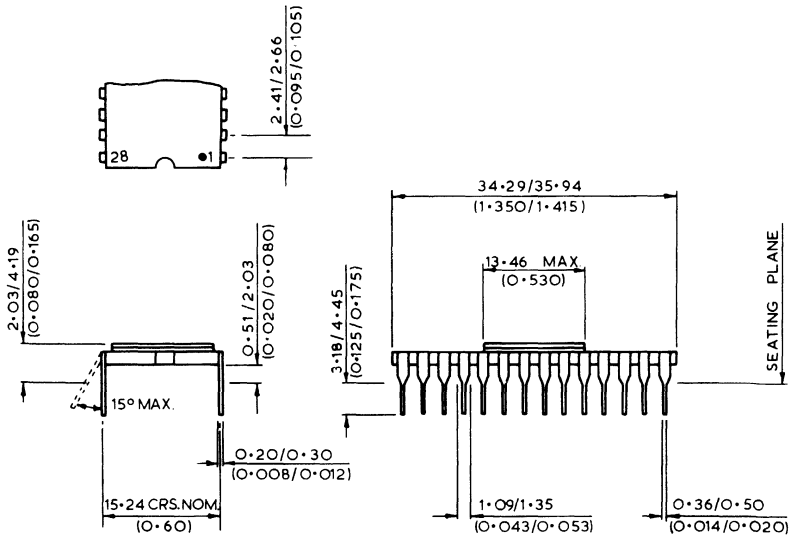


16 LEAD DILMON DC16



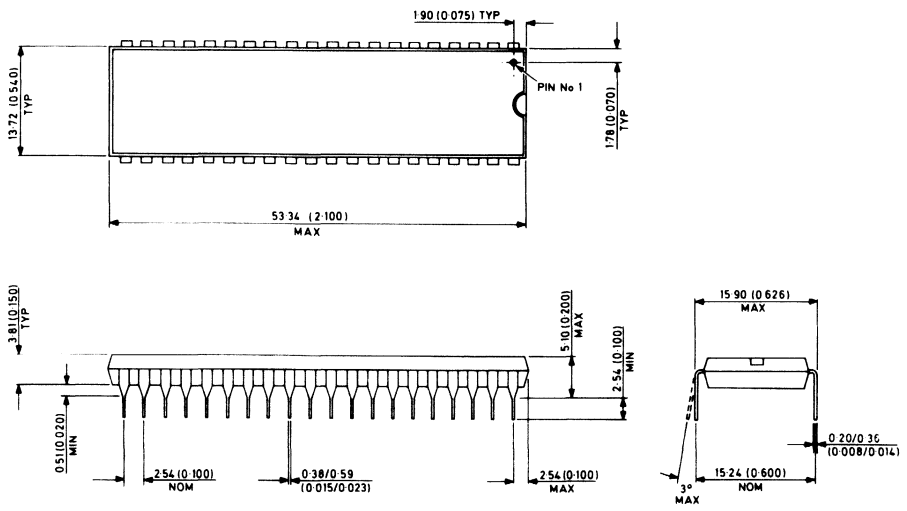
18 LEAD DILMON

DC18



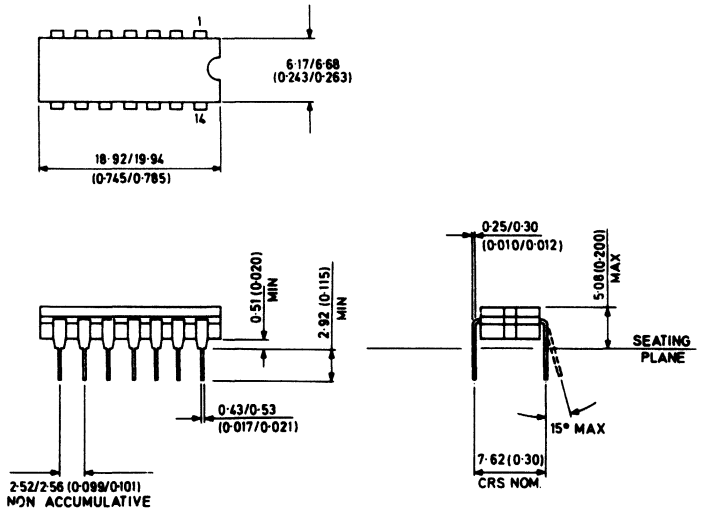
28 LEAD DILMON

DC 28



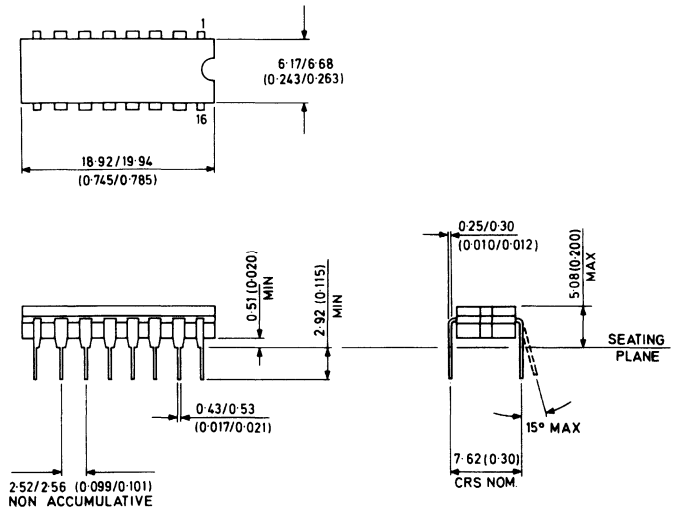
40 LEAD (SIDE BRAZED) DIL

DC40



14 LEAD CERAMIC DIL

DG14



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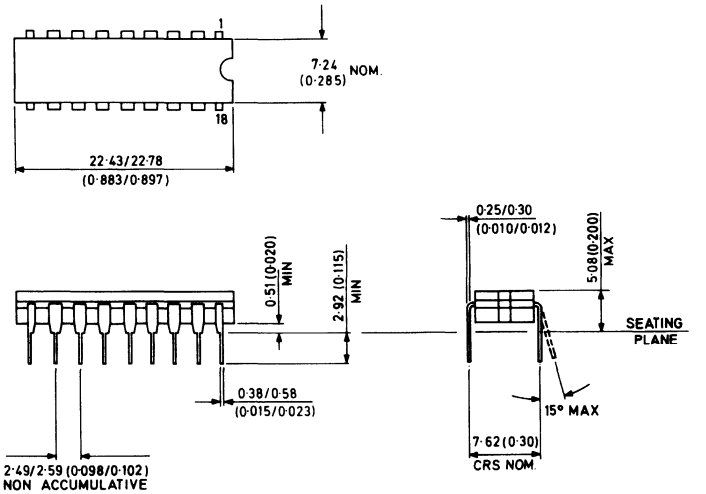

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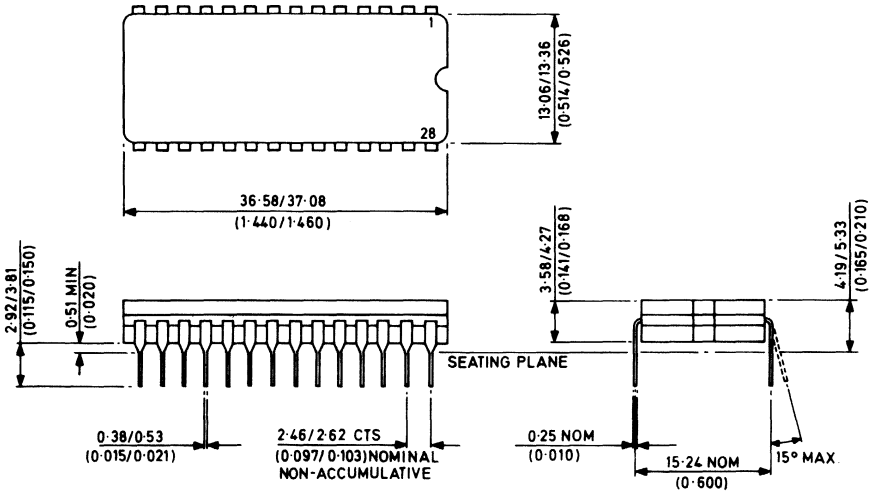

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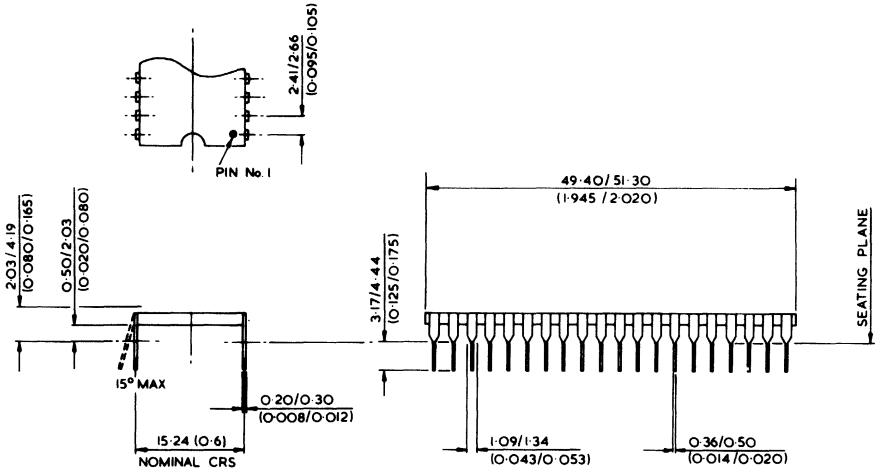

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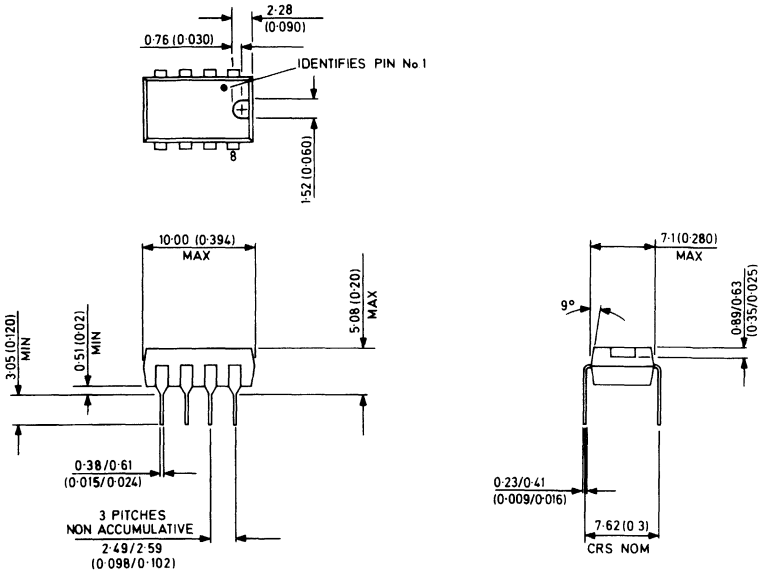

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